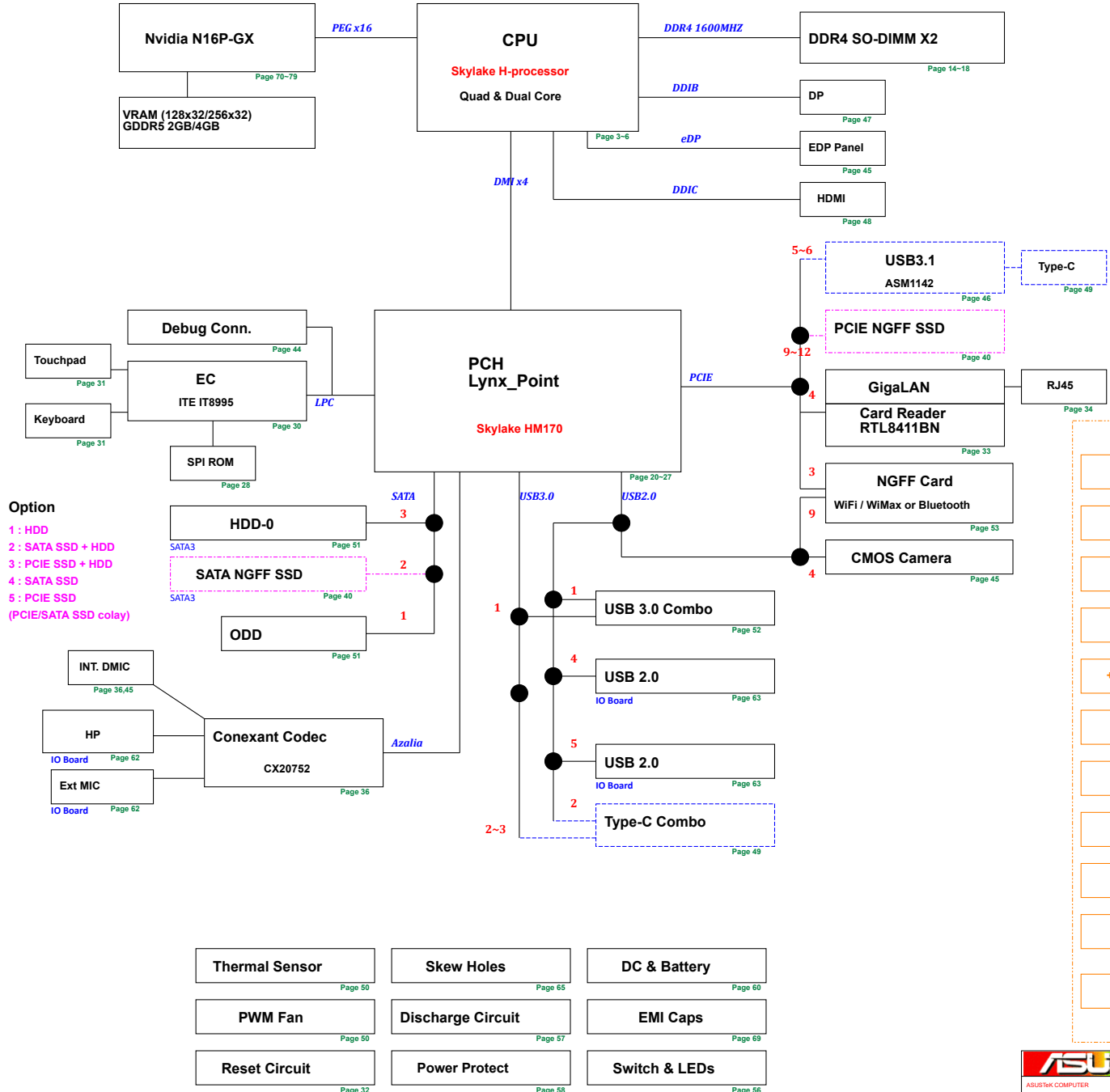


- 001_Block Diagram
002_System Setting
003_CPU_DMI,PEG,eDP,DDI
004_CPU_DDR4
005_CPU_GND
006_CPU_CFG,RSVD
007_CPU_XDP
008_CPU_PWR
009_CPU_PWR
010_CPU_POWER_CAP
014_DIM_DDR4 SO-DIMM A(0) TOP
015_DIM_DDR4 SO-DIMM B(0) TOP
018_DIM_CA/DQ Voltage
020_PCH_HDA,SMBUS,SYS PWR,JTAG
021_PCH-CPT(2)_PCIE,USB2,MISC
022_PCH-CPT(3)_CLK,LPC,USB3
023_PCH-CPT(4)_eDP,PCI,DP
024_PCH-CPT(5)_SPI
025_PCH-CPT(6)_GPIO
026_PCH-CPT(7)_POWER,GND
027_PCH-CPT(8)_POWER,GND
028_PCH-SPI ROM,OTH
029_PCH-XDP
030_KBC_IT8995
031_KBC_KB & TP
032_RST_Reset Circuit
033_LAN_CR_RTL8411BN
034_LAN RJ45
036-AUD-CX20752
037-AUD-AMP
038_AUD-SPEAKER Connector
040_NGFF_SSD
044_DEBUG_LPC
045_eDP
046_USB 3.1 ASM1142
047_DDI_miniDP
048_DDI_HDMI
049_USB 3.1 MB Type-C
050_FAN_Thermal Sensor & Fan
051_HDD & ODD CON
052_USB_Port
053_WiFi/WiMax
056_LED
057_DSG_Discharge
058_Power Protect
059_MB_to_I/O_CONN.
060_DC & BAT IN
062_>>>>>I/O board(1)_MIC/HP
063_>>>>>I/O board(2)_USB
064_>>>>>I/O board(3)_LID SW
065_ME_NUT
069_OTH_EMI
070_VGA_PCI-EXPRESS(1)
071_GPU_FB-IF_GDDR5(2)
072_FRAME BUFFER-A(3)
073_FRAME BUFFER-B(4)
074_VGA_CRT/LVDS(5)
075_VGA_GPIO/DVI/DP(6)
076_VGA_XTAL/STRAPPING(7)
077_VGA_PWG/GND(8)
078_VRAM Cap
080_PW_SKYLAKE (1)
081_PW_SKYLAKE (2)
083_PW_+1.0VSUS
086_PW_1.2V/+VTT/2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD
092_PW_+PEX_VDD
093_PW_+FBVDDQ

GL752VW Block Diagram

Skylake Platform



	Function
15	USB D+D-
14	
13	
12	Camera
11	
10	USB D+D-
9	
8	BT/WLAN
7	
6	
5	

EDS 544924
table 2-17

R0.1-25

+VCCIO



R0301 close to CPU
PEG_COMP trace length <400mils

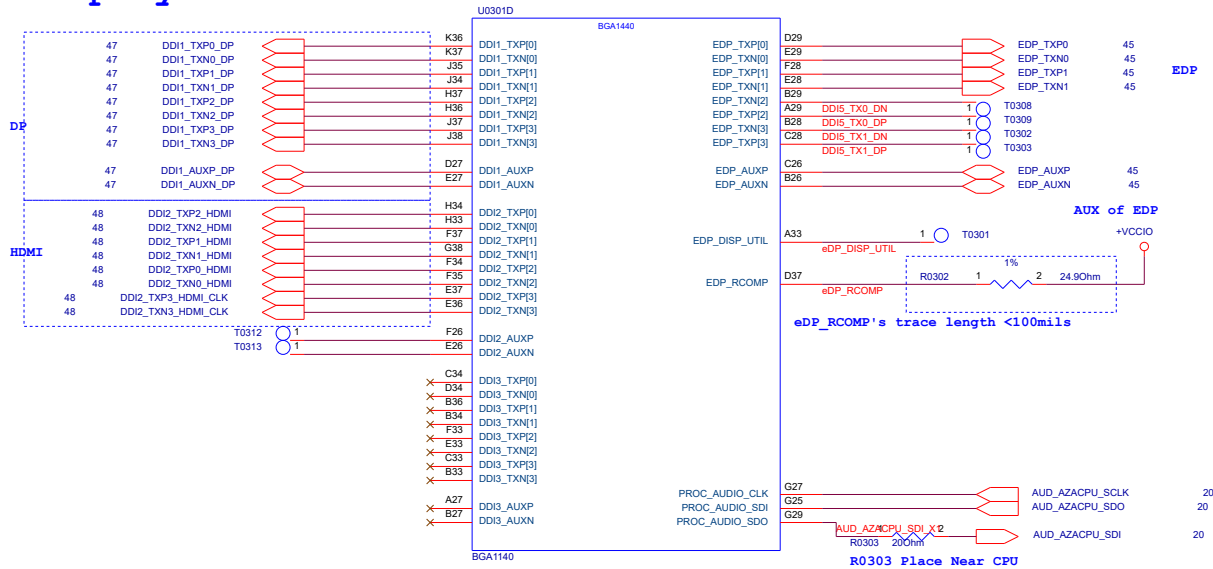
R0.1-25

CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8

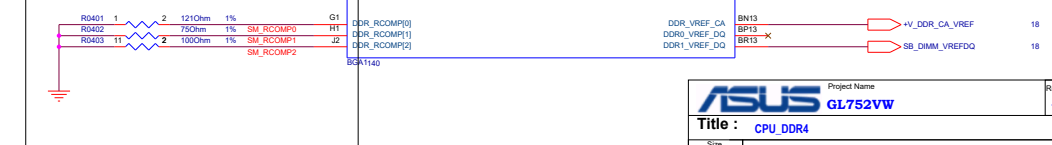
PCIENB_TXN8	CX0309	1	2	0.22UF/6.3V	PCIENB_RXN7
PCIENB_TXN9	CX0310	1	2	0.22UF/6.3V	PCIENB_RXN6
PCIENB_TXN10	CX0311	1	2	0.22UF/6.3V	PCIENB_RXN5
PCIENB_TXN11	CX0312	1	2	0.22UF/6.3V	PCIENB_RXN4
PCIENB_TXN12	CX0313	1	2	0.22UF/6.3V	PCIENB_RXN3
PCIENB_TXN13	CX0314	1	2	0.22UF/6.3V	PCIENB_RXN2
PCIENB_TXN14	CX0315	1	2	0.22UF/6.3V	PCIENB_RXN1
PCIENB_TXN15	CX0316	1	2	0.22UF/6.3V	PCIENB_RXN0

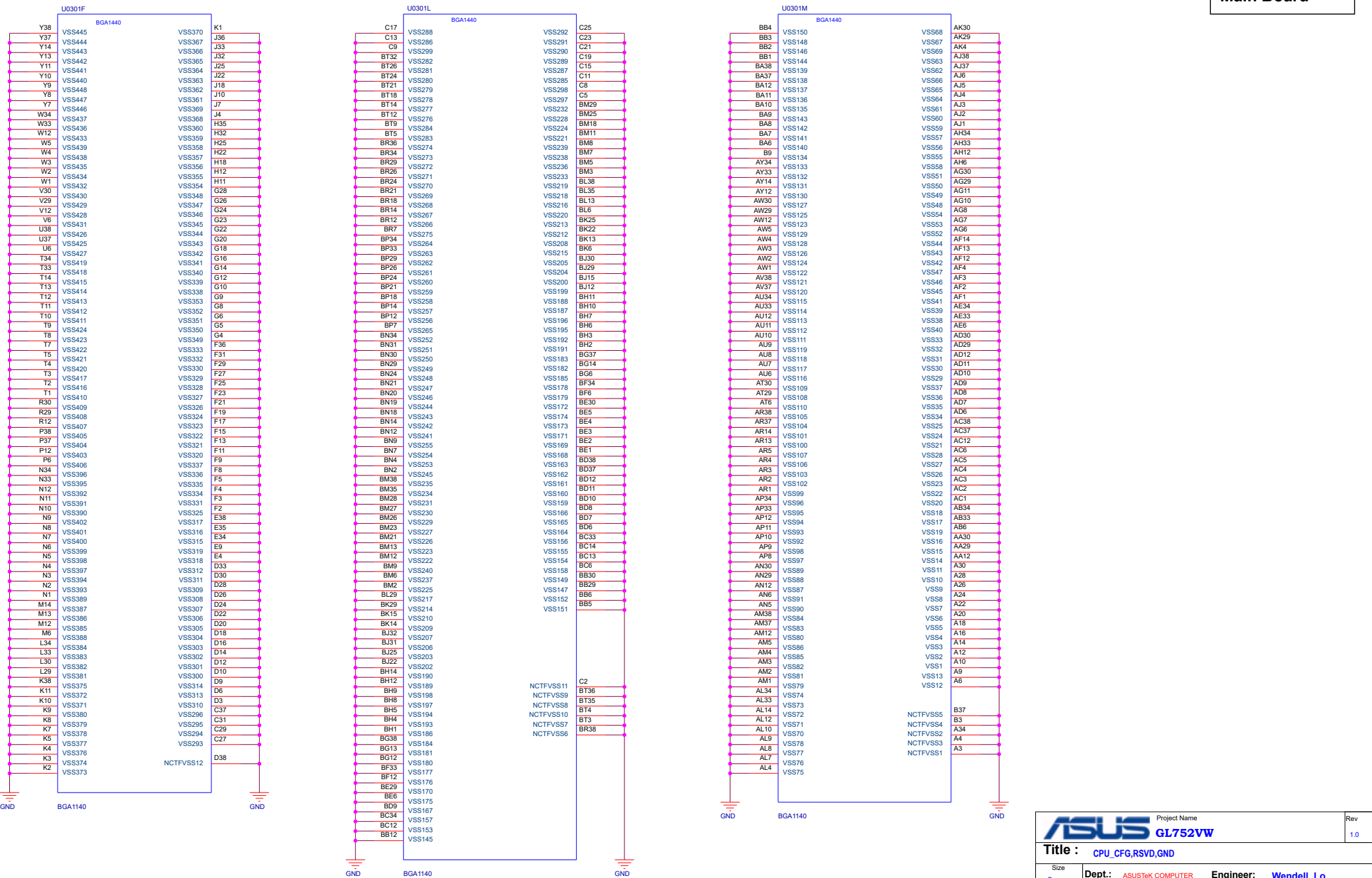
PCIENB_TXP8	CX0325	1	2	0.22UF/6.3V	PCIENB_RXP7
PCIENB_TXP9	CX0326	1	2	0.22UF/6.3V	PCIENB_RXP6
PCIENB_TXP10	CX0327	1	2	0.22UF/6.3V	PCIENB_RXP5
PCIENB_TXP11	CX0328	1	2	0.22UF/6.3V	PCIENB_RXP4
PCIENB_TXP12	CX0329	1	2	0.22UF/6.3V	PCIENB_RXP3
PCIENB_TXP13	CX0330	1	2	0.22UF/6.3V	PCIENB_RXP2
PCIENB_TXP14	CX0331	1	2	0.22UF/6.3V	PCIENB_RXP1
PCIENB_TXP15	CX0332	1	2	0.22UF/6.3V	PCIENB_RXP0

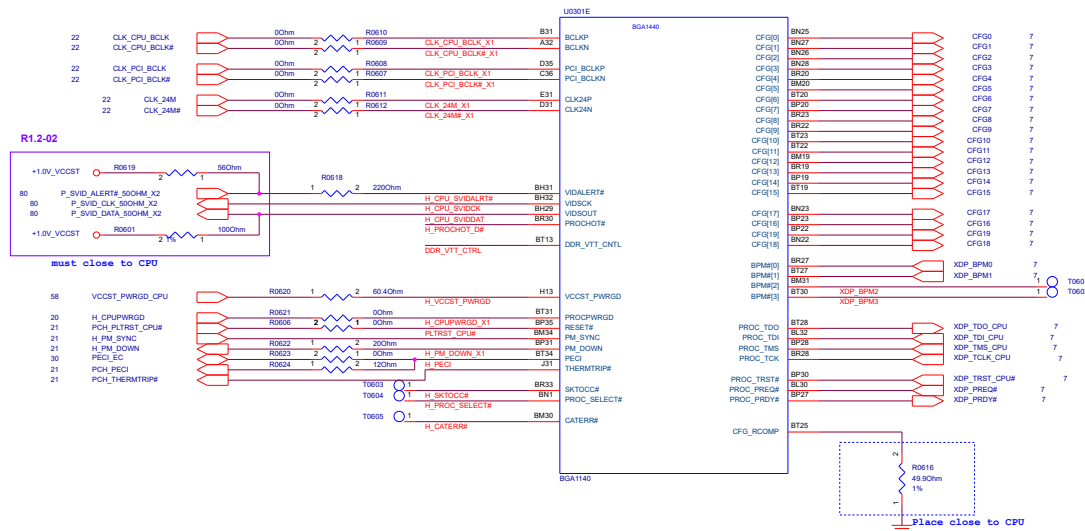
Display



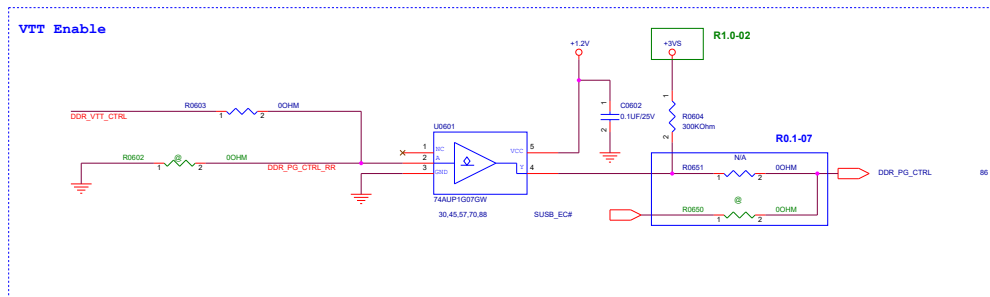
Main Board



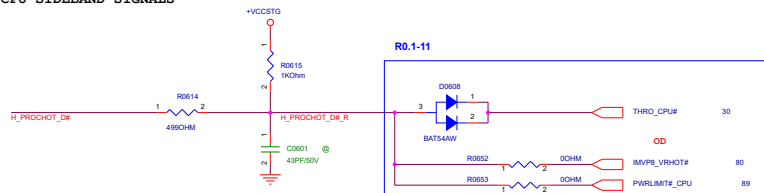




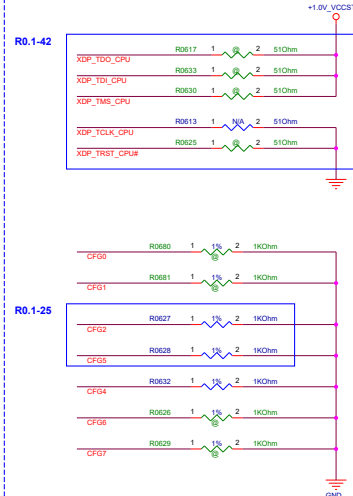
DDR VTT CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924 544924 Skylake EDS Vol 1 Rev0.9.pdf P.120



CPU SIDEBAND SIGNALS



CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
--

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express® Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

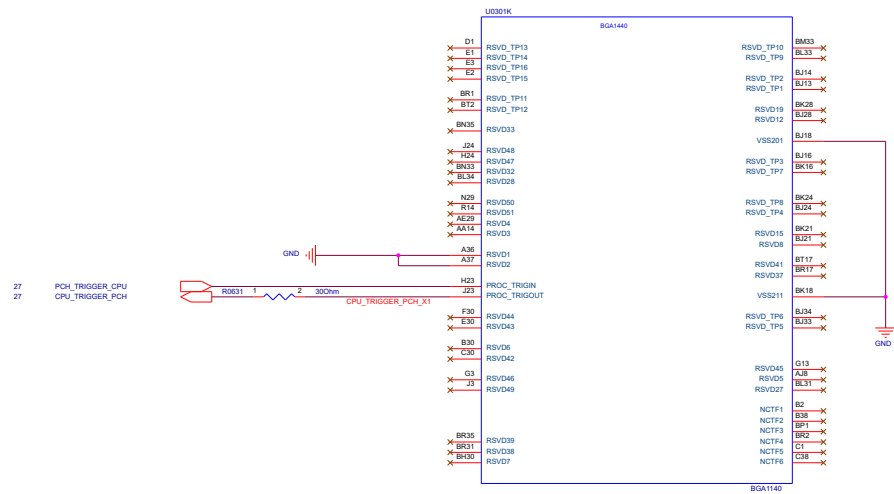
CFG[7] : PEG Training

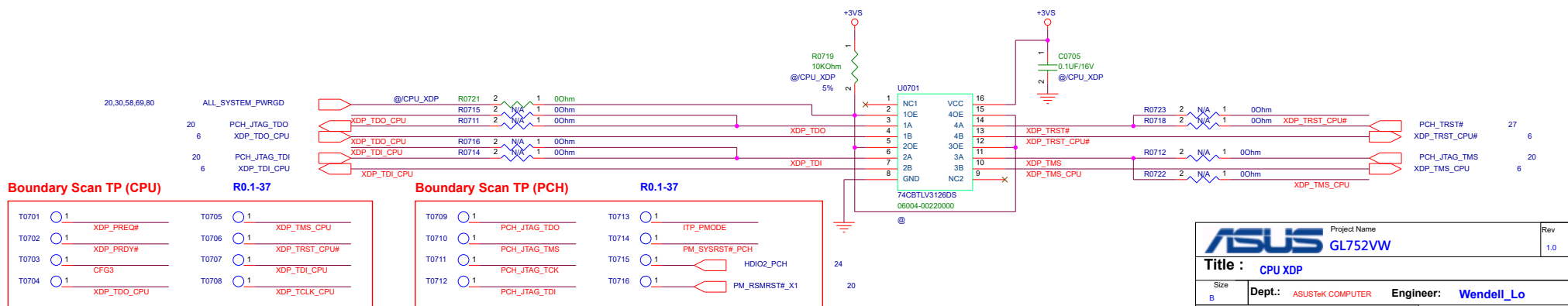
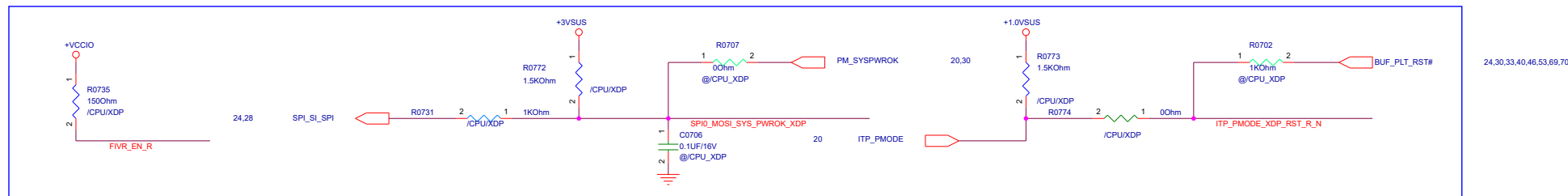
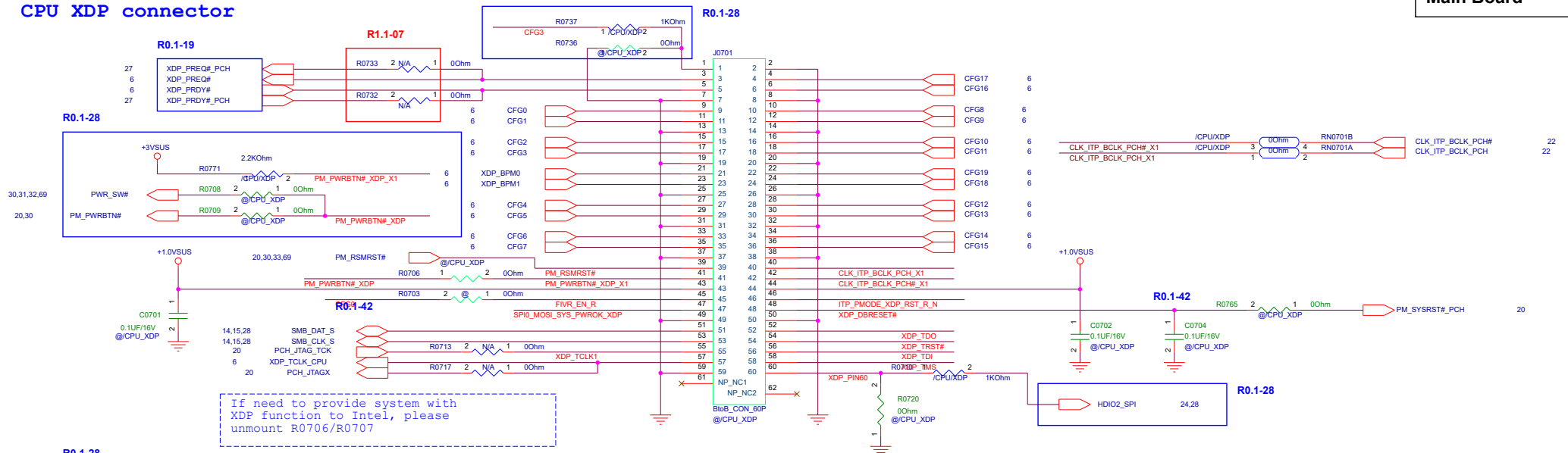
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

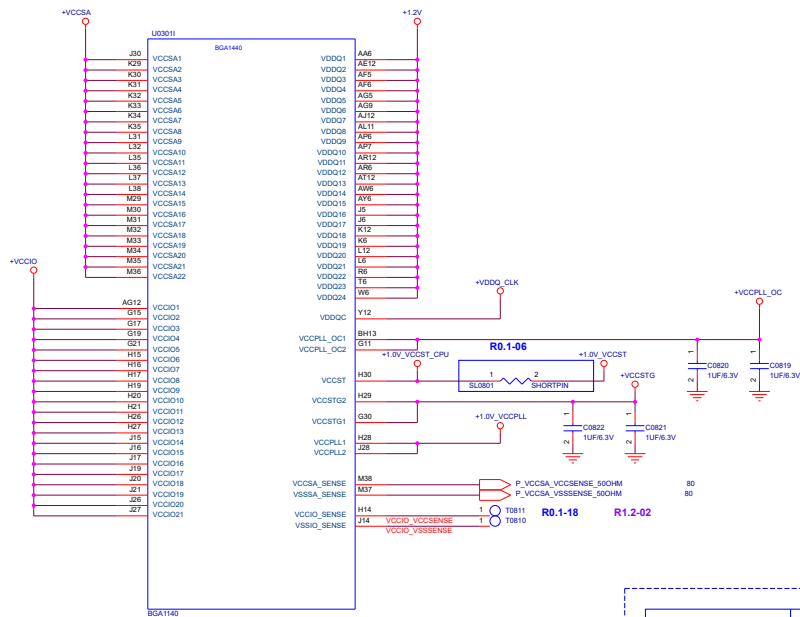
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

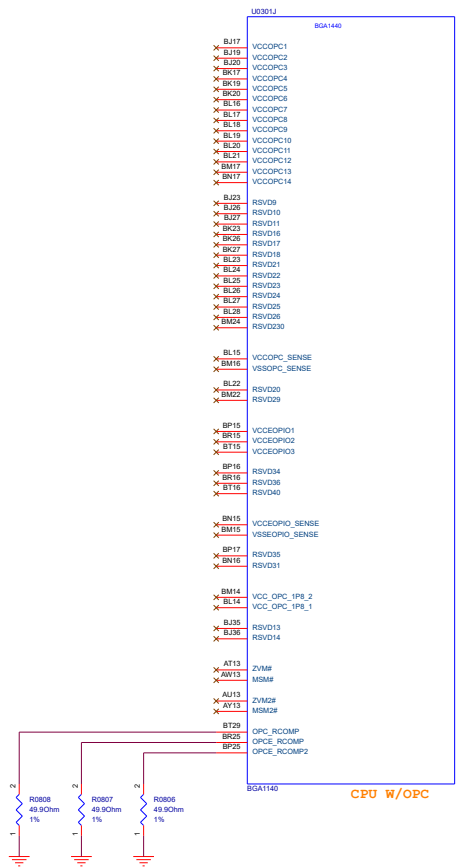
Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 20141209



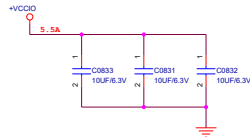




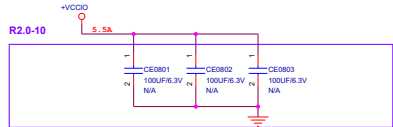
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CPU	+VDDQ_CLK
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	



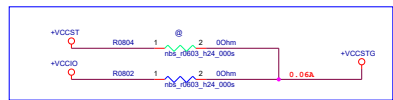
+VCCIO DECAPS Place Back Side (TOP)



+VCCIO DECAPS Place Back Side (BOT)

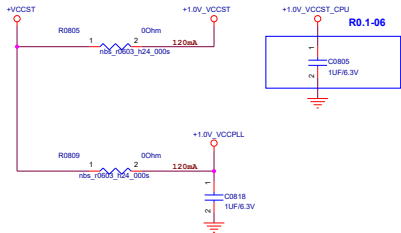


R0.1-06

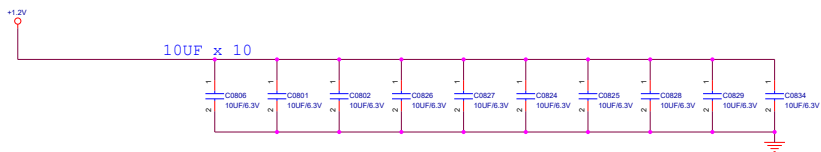


Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

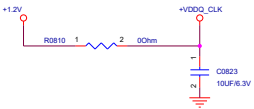
+1.0V_VCCST/+1.0V_VCCPLL
DECAPS Place Back Side (TOP)



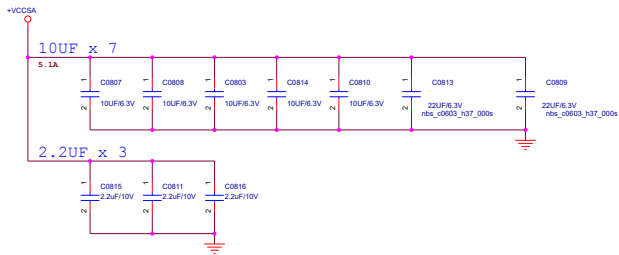
+VDDQ DECAPS Place Back Side (TOP)

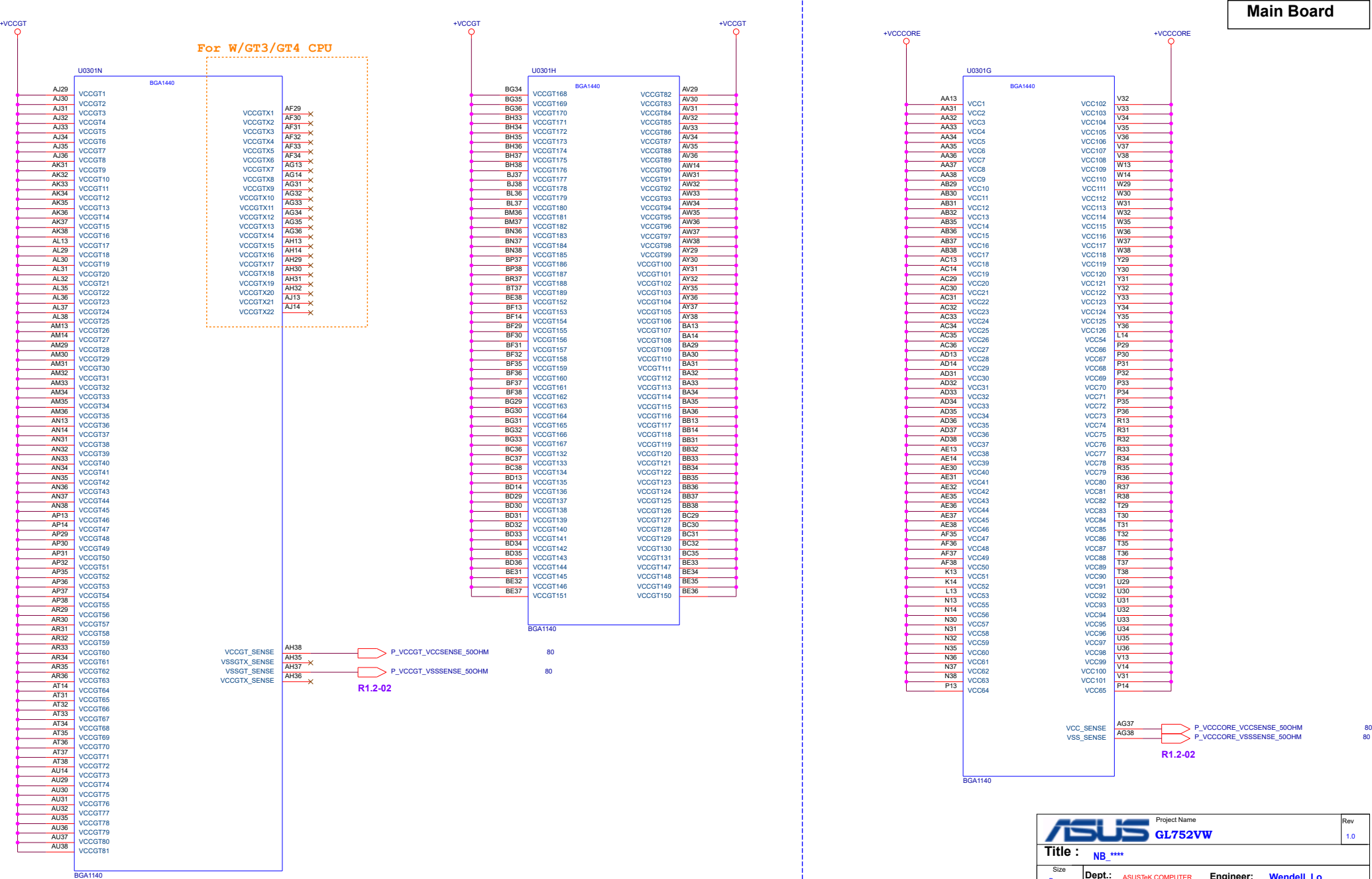


+VDDQ CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)

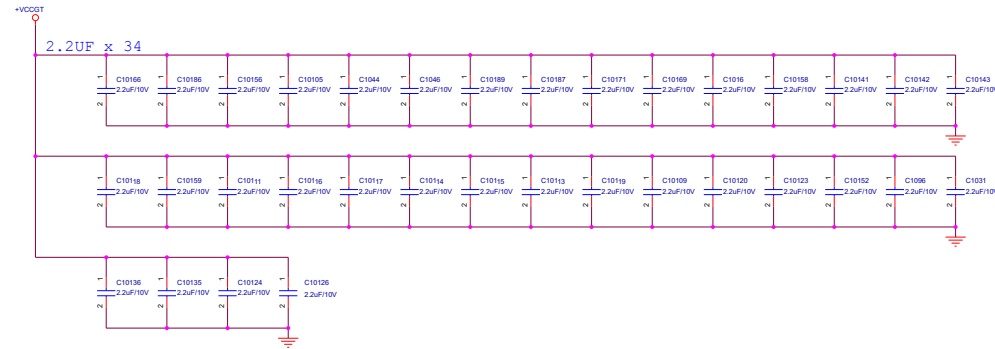
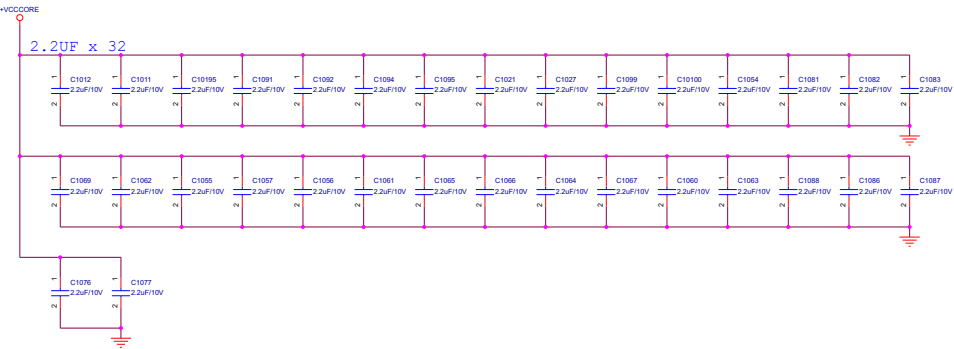
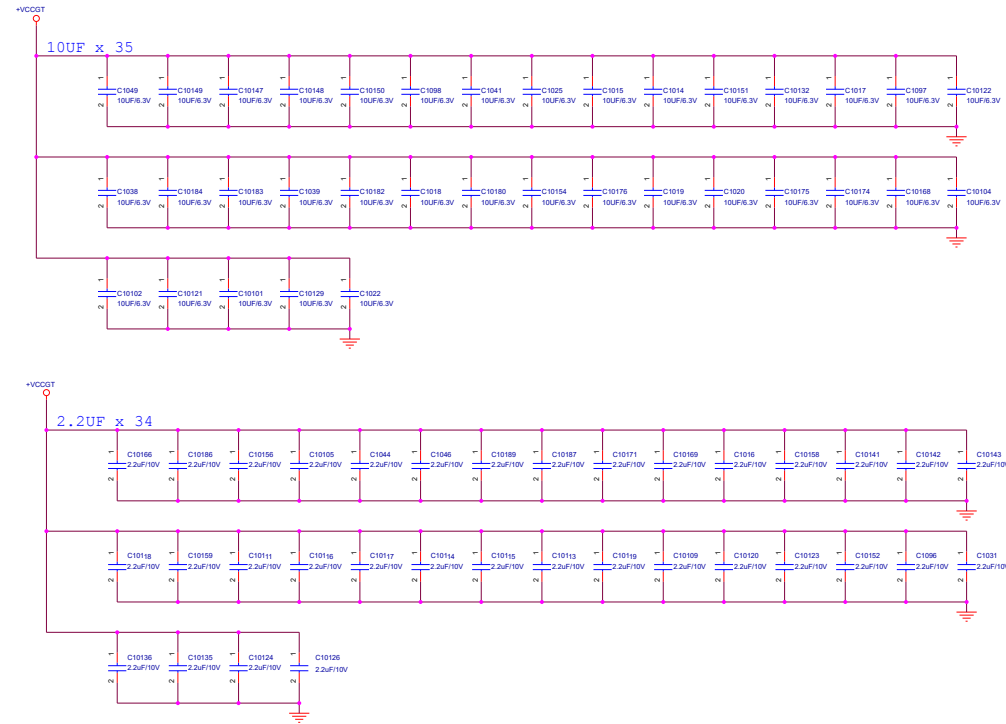




+VCCORE DECAPS Place Back Side (TOP)



+VCCGT DECAPS Place Back Side (TOP)



<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 11 of 102	

<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 12 of 102	

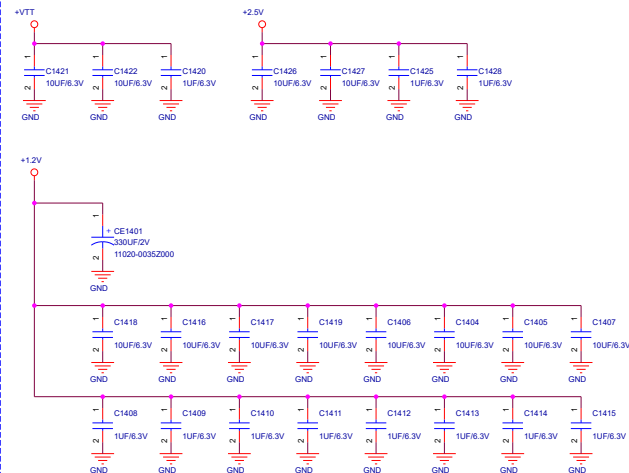
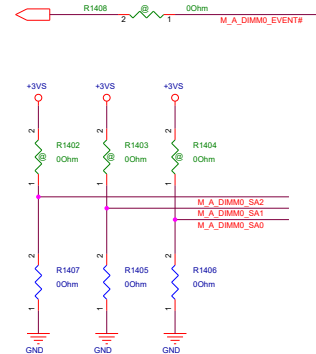
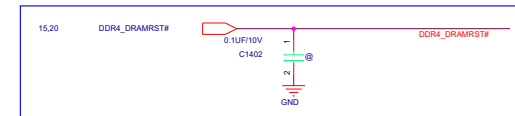
<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 13 of 102	

[illegible]

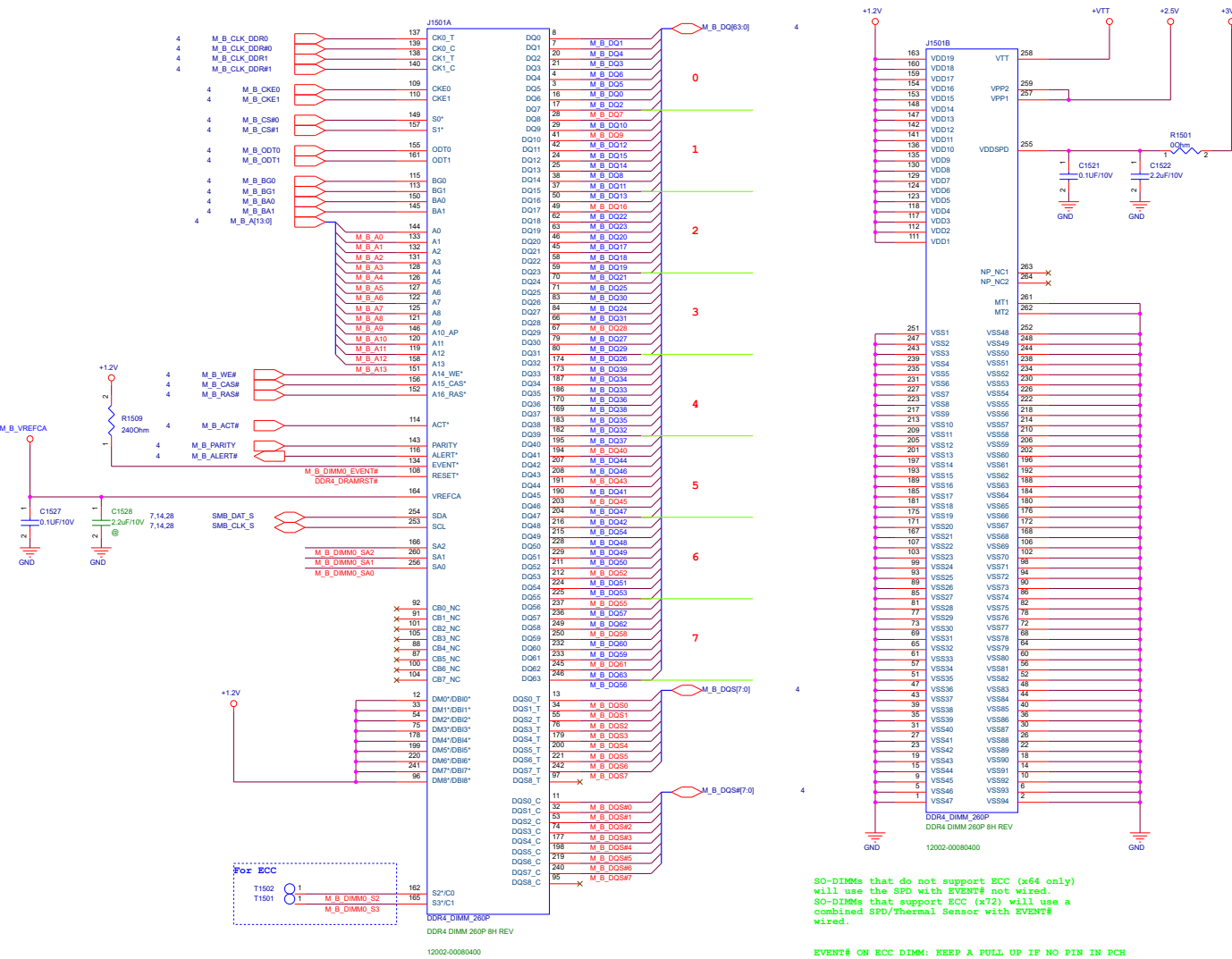
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

R0.1-03



SODIMM CHB-DIMM0
TOP H8.0mm REV (J1501)

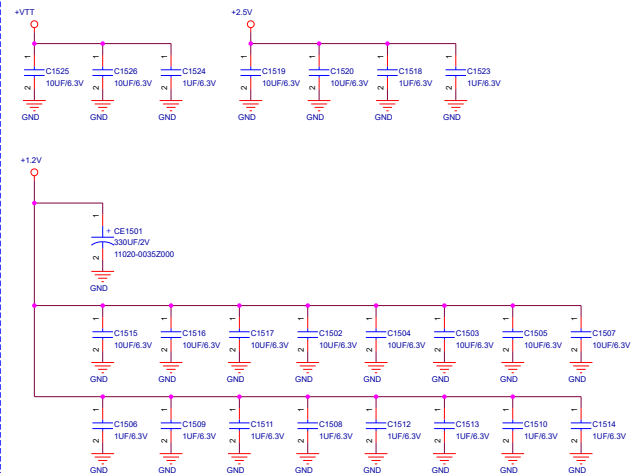
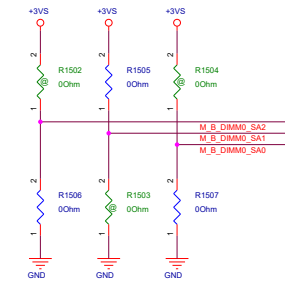
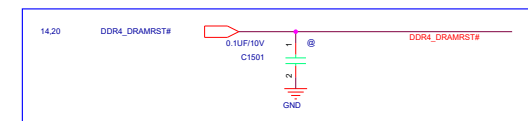
12002-00080400
DDR4 DIMM 260P 8H REV



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

R0.1-03



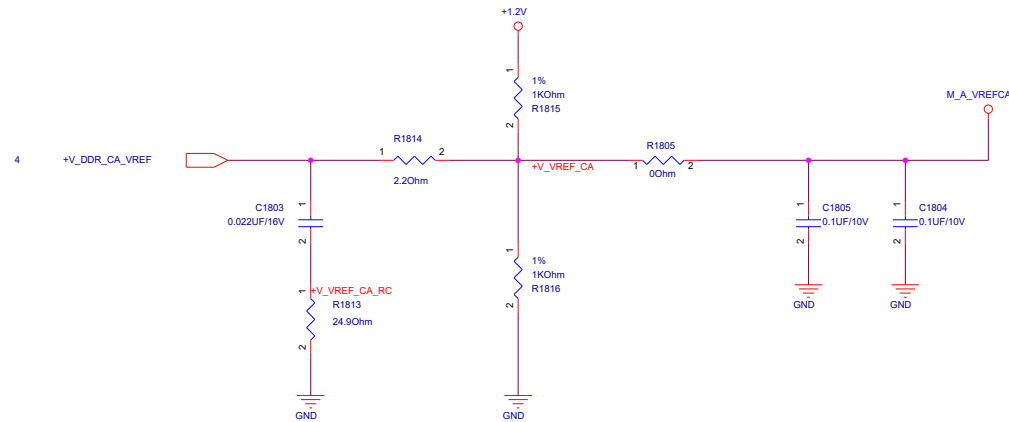
<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 16 of 102	

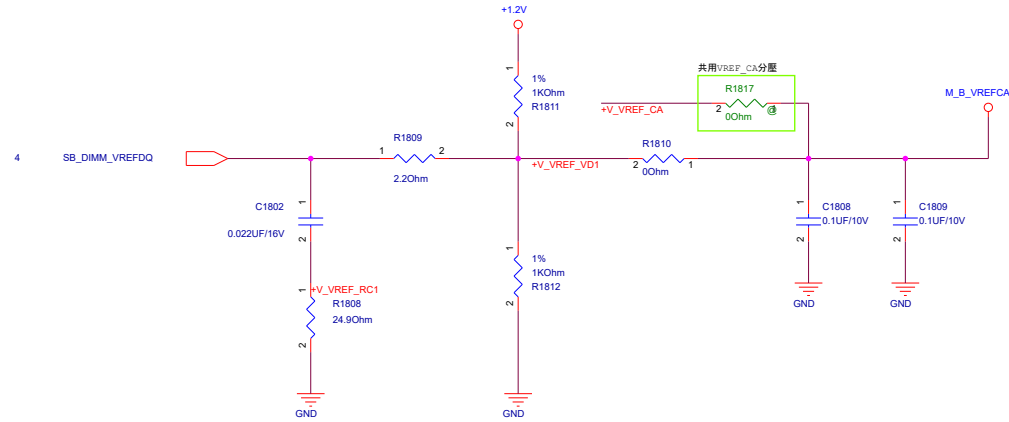
<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 17 of 102	

SO-DIMM0 Vref



SO-DIMM1 Vref



		Title : Green CLK Gen	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	Rev	
A	GL752VW	1.0	
Date: Wednesday, September 23, 2015		Sheet	19 of 102

HD Audio



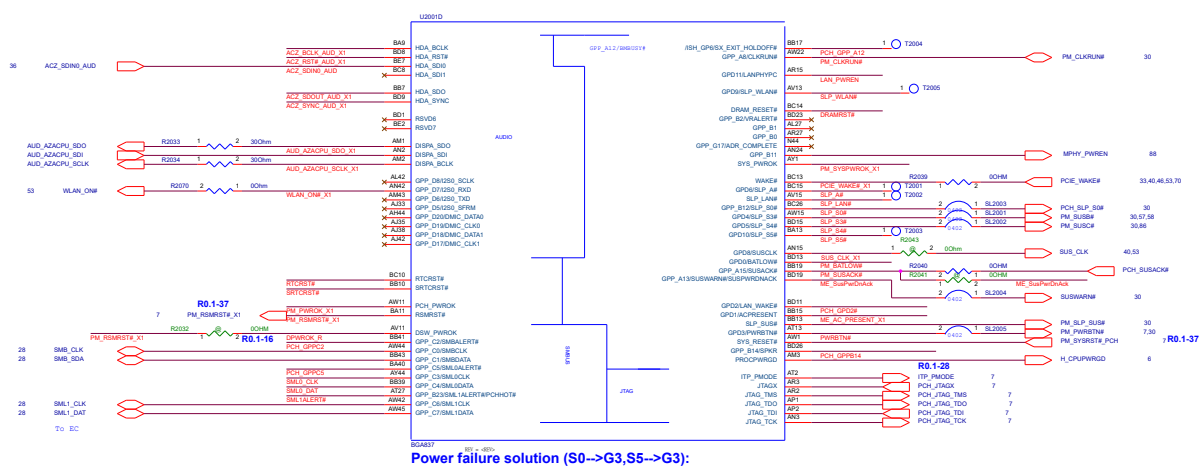
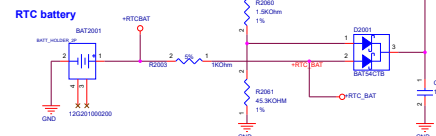
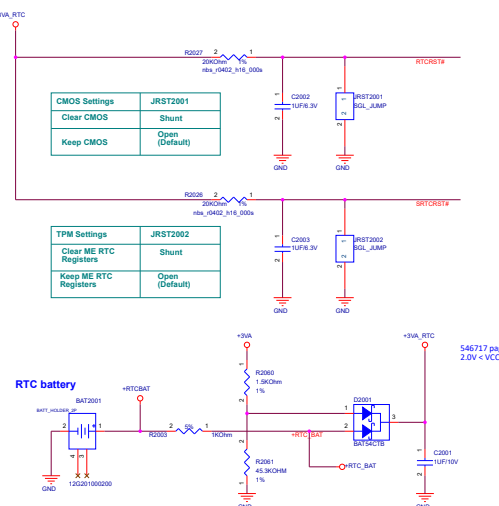
HDA_SYNC (On-Die PLL VR voltage select):
Rising edge of RSMRST# pin
High:1.5V, Low:1.8V (default)



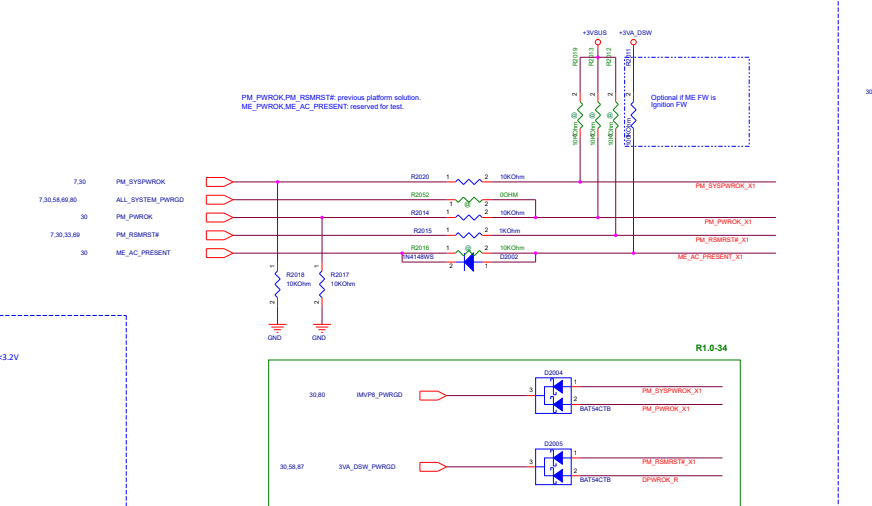
ACZ_SDOU:
(1) PCH:
Internal PD 20k ohm,
VIL=0.35V, VIH=0.65~3.3V
(2) ALC2691:
VIL<0.35~3.3V, VIH>0.65~3.3V

ACZ_SDOU is a signal used for Flash
Descriptor security override/RE debug mode
HIGH : get override, LOW : disable override

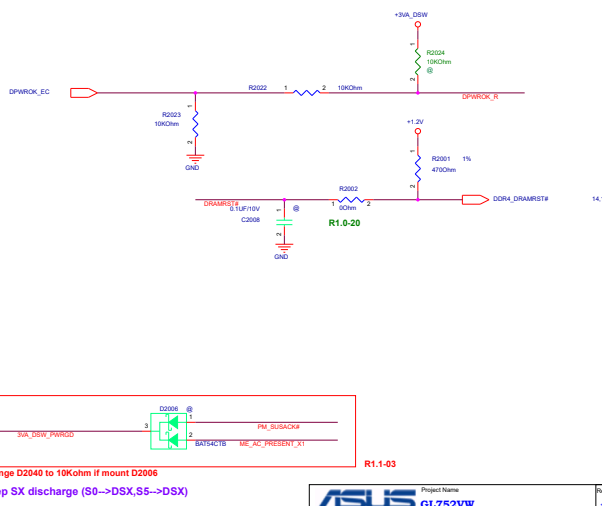
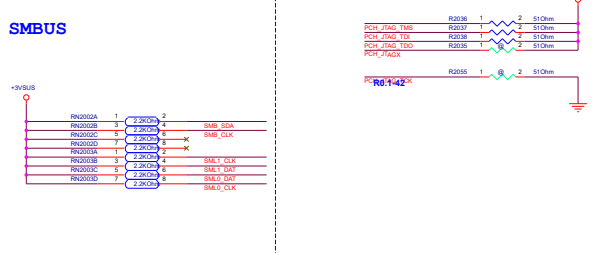
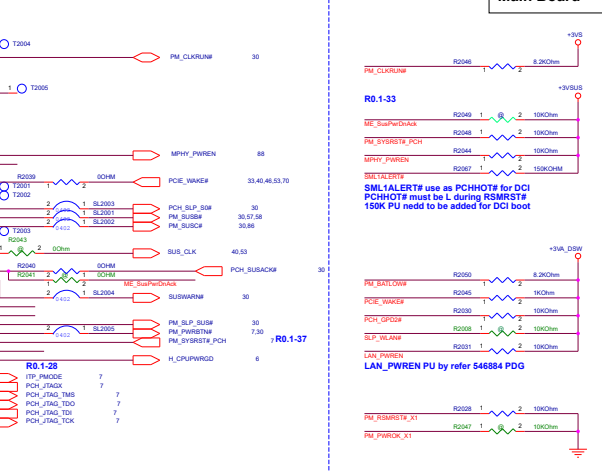
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO



eSPI or LPC	TLS Confidentiality	Top Swap Override
+3V3US	+3V3US	+3V3US
PCH_GPPC2	PCH_GPPC2	PCH_GPPC2
PCH_GPPC3: weak internal pull down	PCH_GPPC2: weak internal pull down	PCH_GPPC14: weak internal pull down
PU eSPI	PU Enable	PU Enable
PD LPC (default)	PD Disable (default)	PD Disable (default)



Power failure solution (S0-->G3,S5-->G3)



Change D2040 to 10Kohm if mount D2006
Deep SX discharge (S0-->DSX,S5-->DSX)

Main Board

must close to PCH



Title : LAN_*****

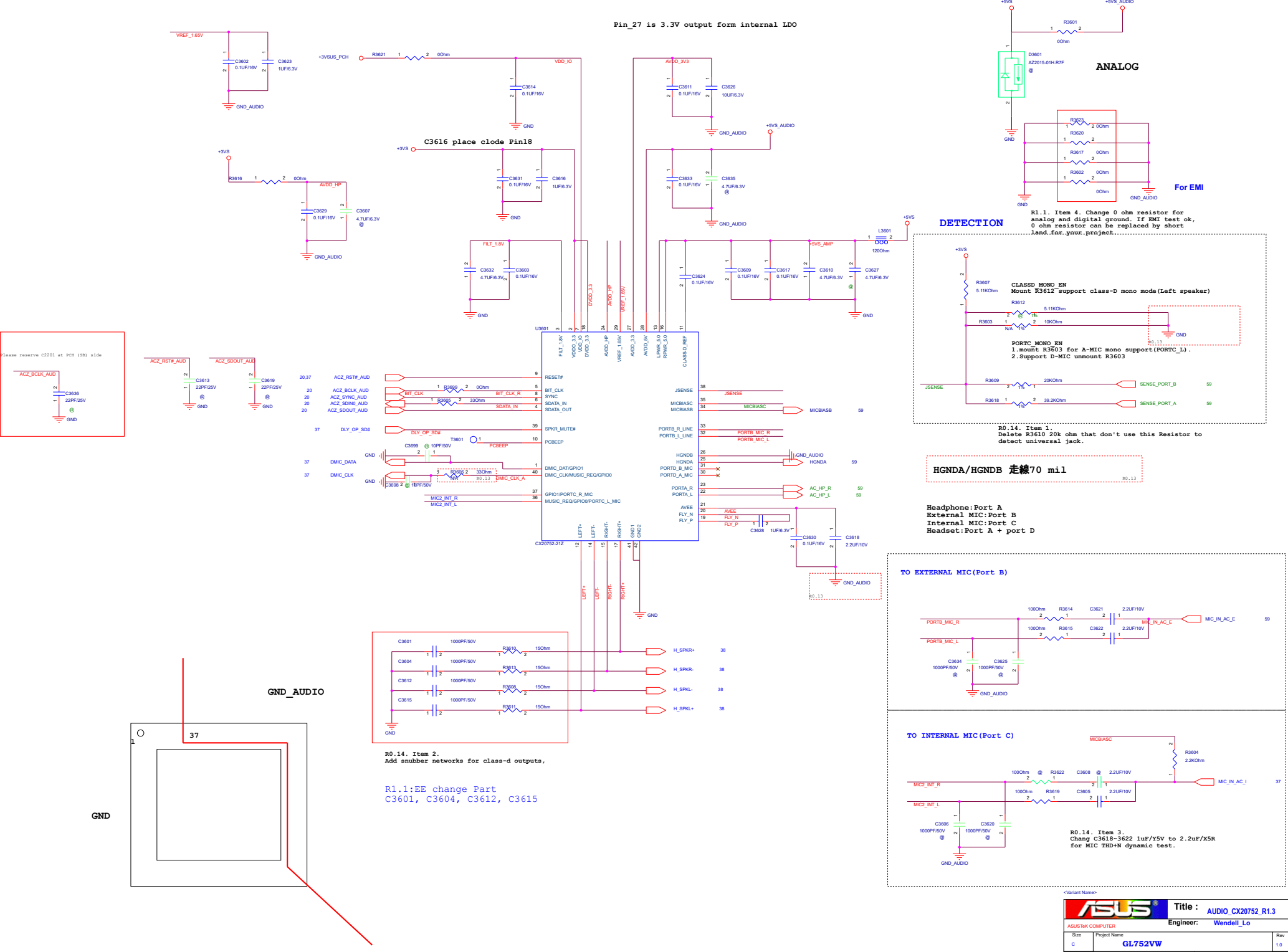
ASUSTeK COMPUTER

Engineer: Wendell_Lo

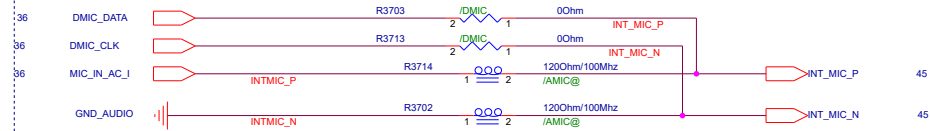
Size	Project Name
B	GL752VW

Rev
1.0

Pin_27 is 3.3V output form internal LDO

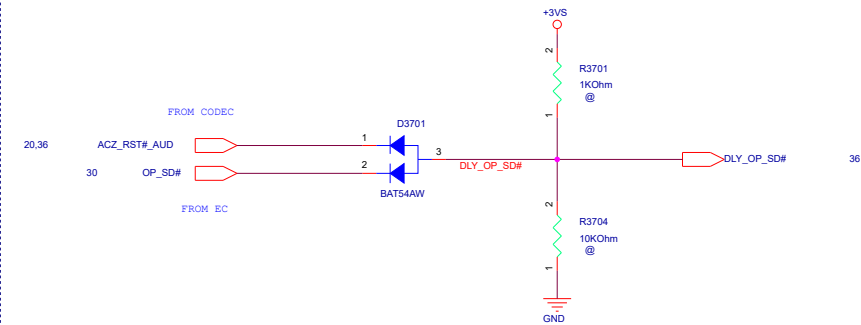


INTERNAL MICROPHONE



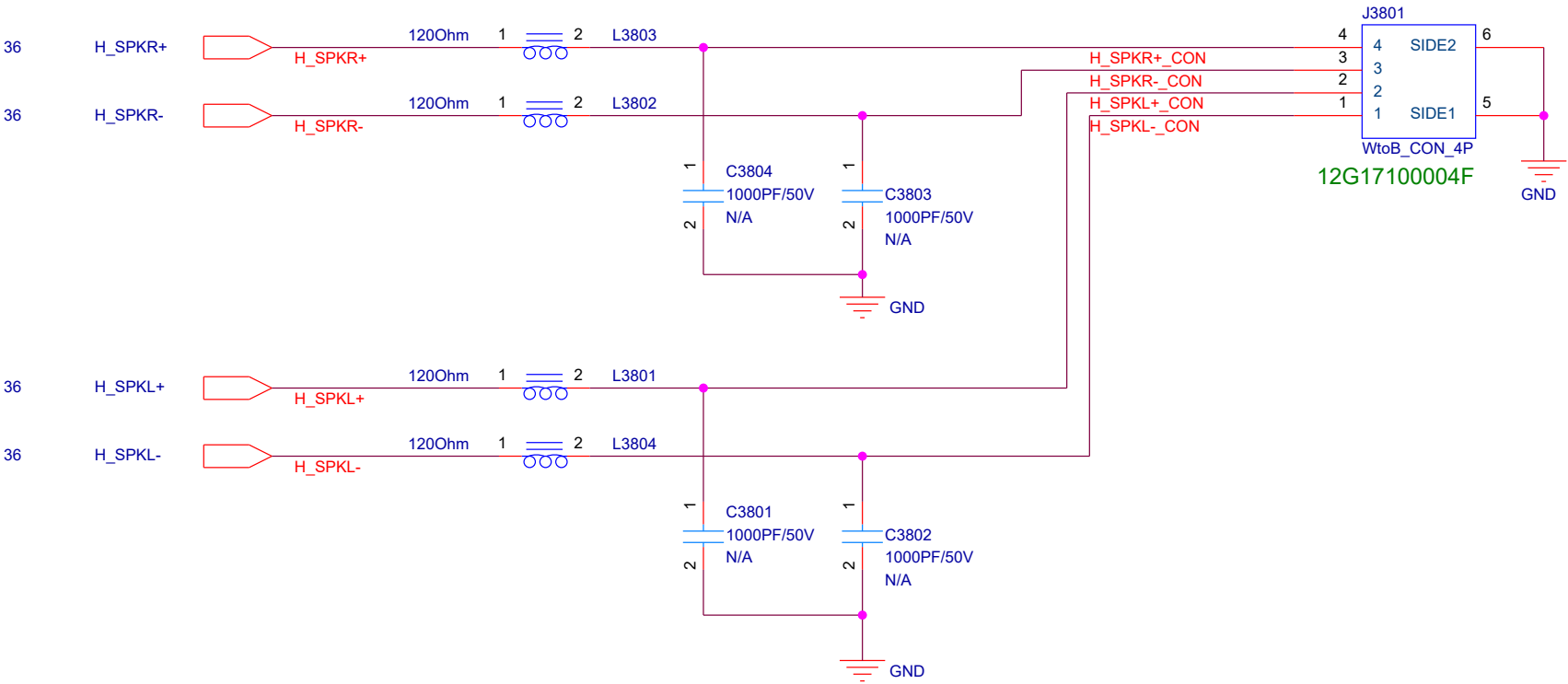
R2.0 change change R3714,R3702 from R to bead

MUTE CONTROL



<Variant Name>

PART NO	IMPEDANCE (Ω) AT100 MHz 500mV	DC RESISTANCE (Ω) Max	RATED CURRENT (mA) Max
ACMS160808A121 RDC05	120±25%	0.05	3000



<Variant Name>

		Title : AUD-MIC-IN__R1.4	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 38 of 102	



Title : **AUD_WOOFER**

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size

Project Name

Rev

B

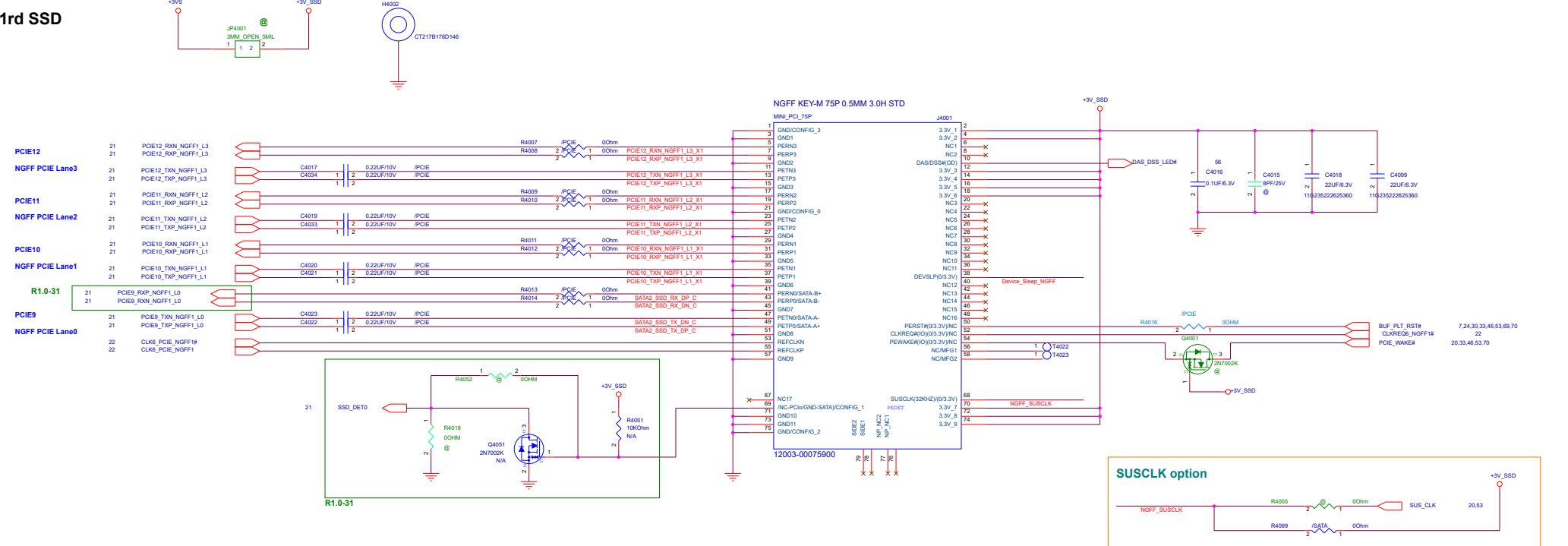
GL752VW

1.0

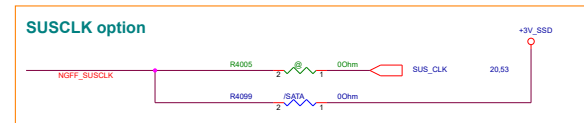
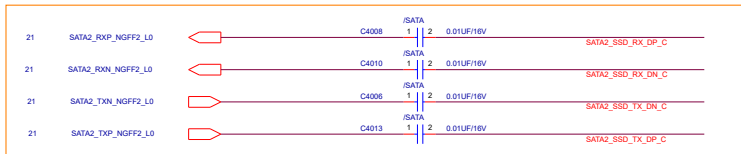
Date: Wednesday, September 23, 2015

Sheet 39 of 102

1rd SSD



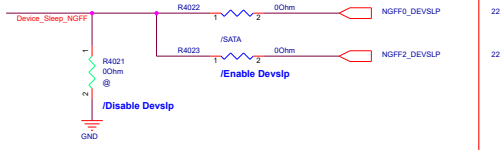
SATA SSD



R1.1-05 **R0.1-43**

HW_Control NGFF Device Sleep

Close to Device connector



HW Disable SSD Devslp	Mount R4021=0ohm, Unmount R4022 and R4023=0ohm
HW Enable SSD Devslp	Unmount R4021=0ohm, Mount R4022 or R4023=0ohm



Title : CLK_GEN

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name
B	GL752VW

Rev
1.0



Title : CB_RTS5139

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name
B	GL752VW

Rev
1.0



Project Name

GL752VW

Rev

1.0

Title : **DP to VGA_ANX6210**

Size

B

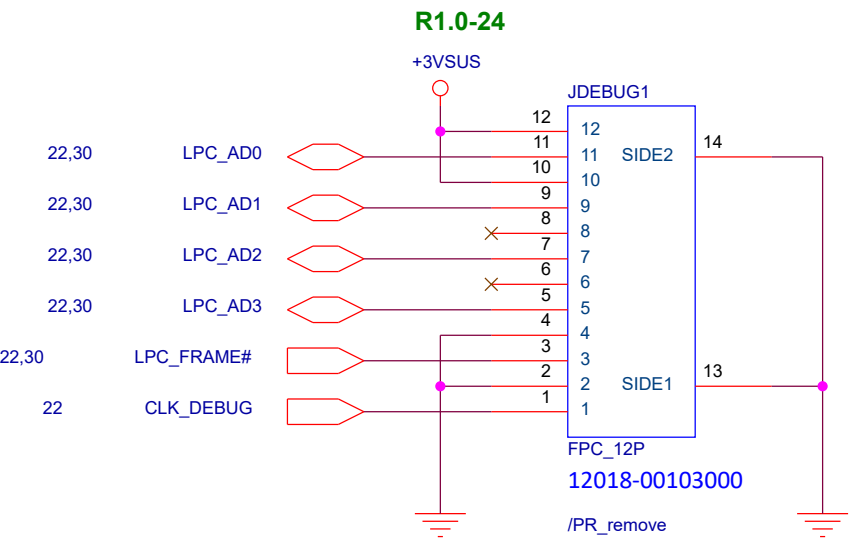
Dept.: **ASUSTeK COMPUTER**

Engineer: **Wendell_Lo**

Date: **Wednesday, September 23, 2015**

Sheet **43** of **102**

LPC Debug Port



```
1k ohm resistor (0402) for 5% precise
: 10G212102004010

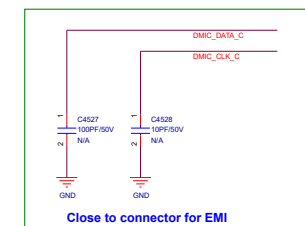
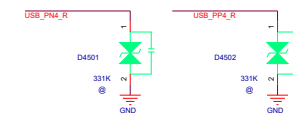
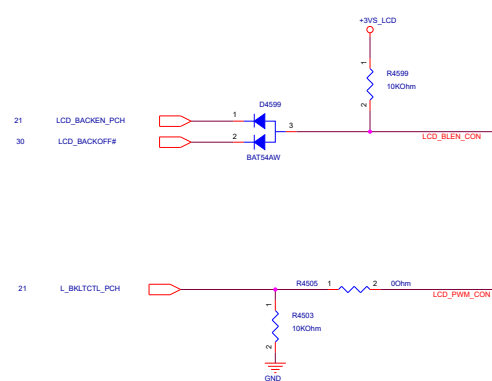
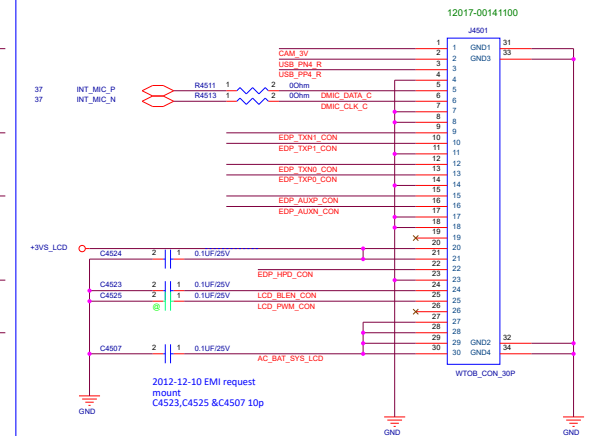
R4597 gives a current limitation for the PCM GPIO
when pin 3 is acted as flag# (103/05/13)
```

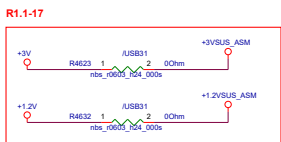


The schematic diagram illustrates the electrical connections for the EDP board. It shows the following components and connections:

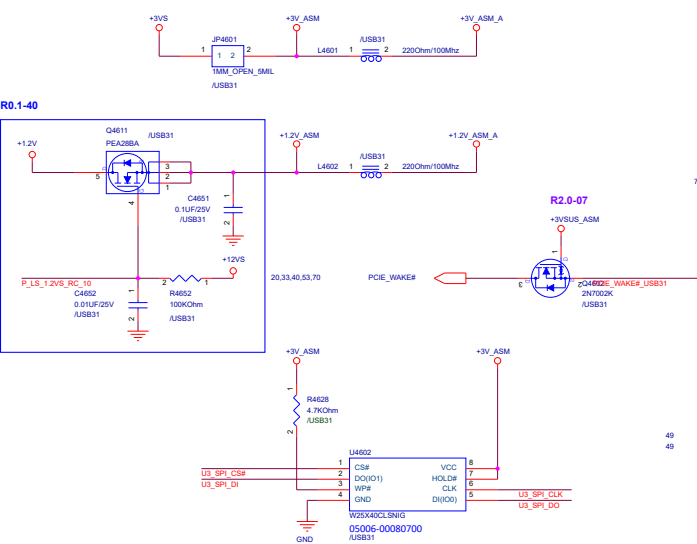
- EDP_TXN0 and EDP_TXP0:** Connected to C4504 and C4505 (0.1uF/6V) which are in turn connected to EDP_TXN0_C and EDP_TXP0_C.
- EDP_TXN1 and EDP_TXP1:** Connected to C4519 and C4513 (0.1uF/6V) which are in turn connected to EDP_TXN1_C and EDP_TXP1_C.
- EDP_ALXP and EDP_ALXN:** Connected to C4520 and C4508 (0.1uF/6V) which are in turn connected to EDP_ALXP_C and EDP_ALXN_C.
- Power and Grounding:** A +3V5 supply is connected to a network of resistors (R4514, R4516, R4501, R4504) and capacitors (R4509, R4508) leading to GND.
- EDP_HPD:** A connection point for the HPD signal, linked to R4588 and a 50kOhm resistor.

The schematic diagram illustrates the USB-PN4 receiver circuit. It features two parallel signal paths for USB_PN4_R and USB_PN4_I. Each path includes a 30ohm resistor, an L-match network (L4514, 500nH/100MHz), and an N4550B diode. The receiver is powered by a +3VS supply through a 300ohm resistor and a 1200nH inductor (L4501) to a C4501 capacitor (0.1uF/18V).

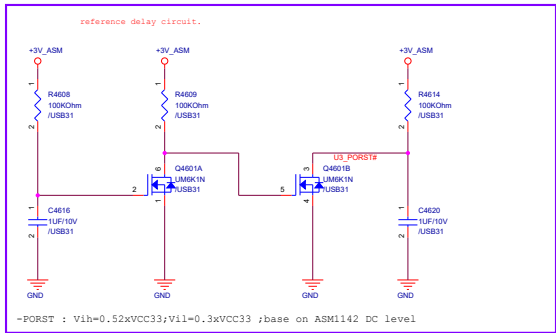
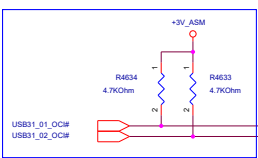
[illegible]



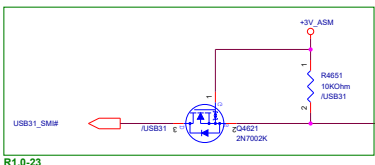
R0.1-40



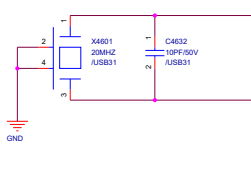
R0.1-21



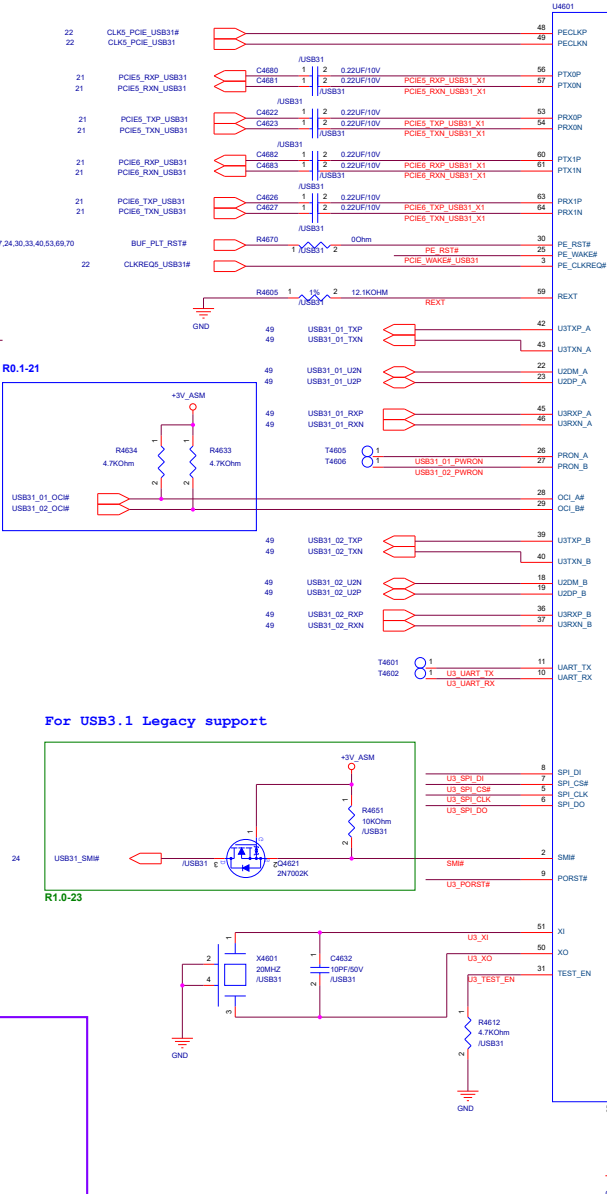
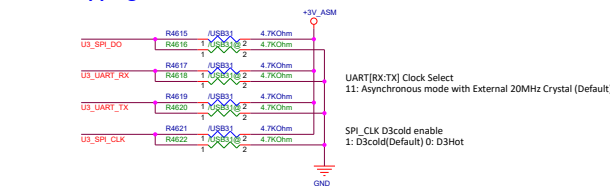
For USB3.1 Legacy support



R1.0-23

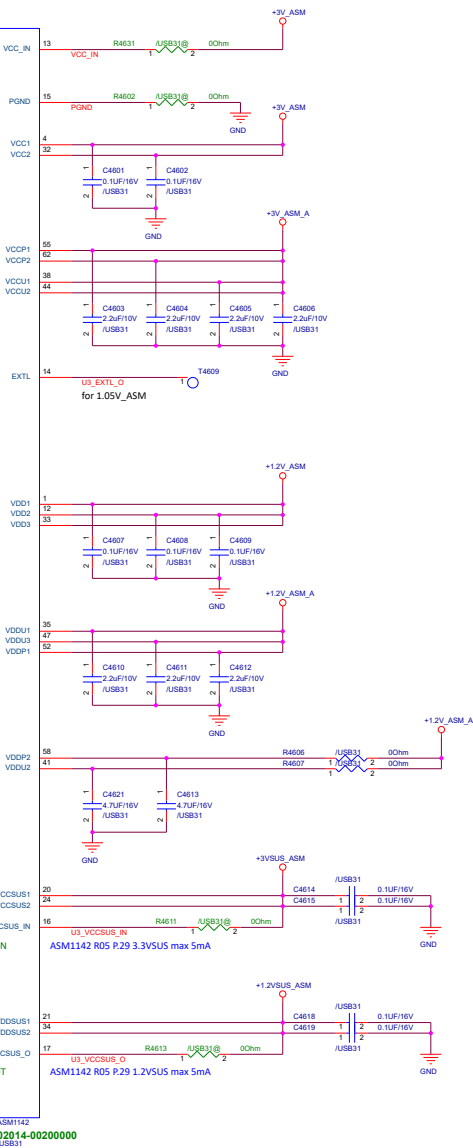


H/W Strapping

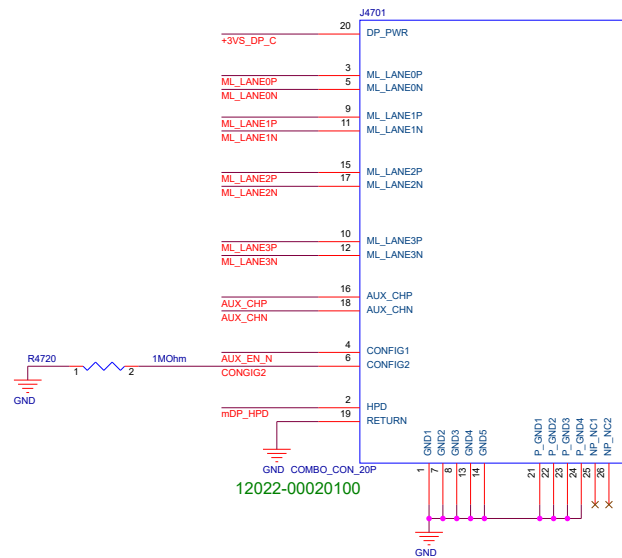
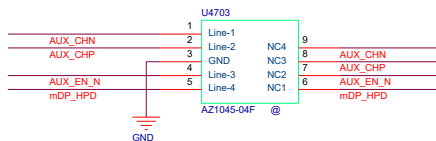
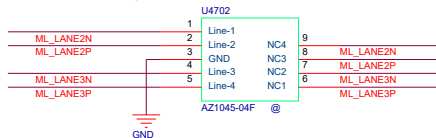
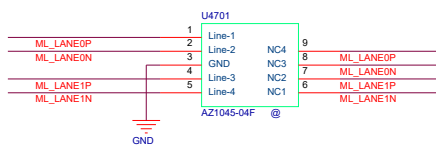
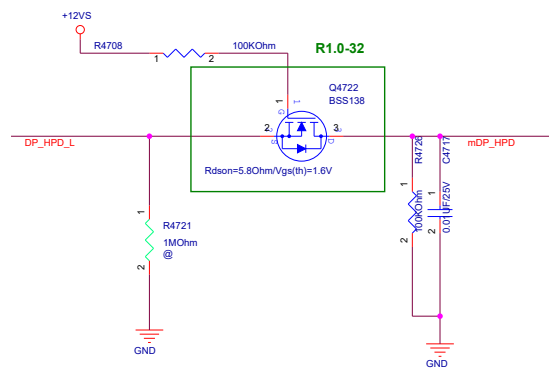
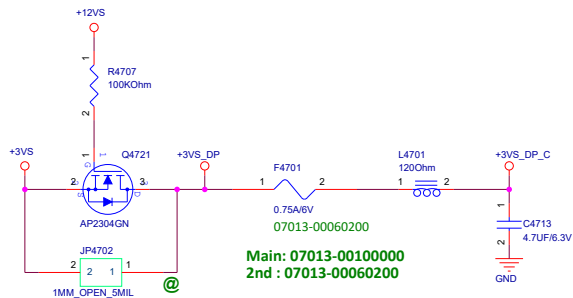
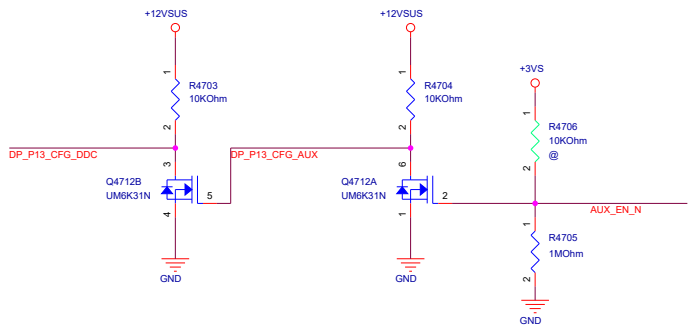
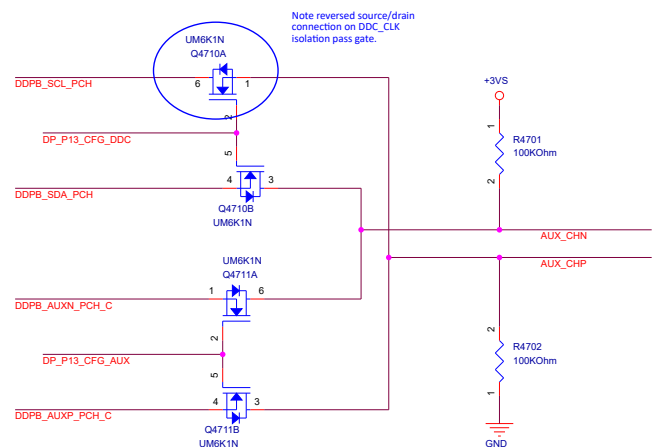


1.05VSUS LDO IN

1.05VSUS LDO OUT



Follow SKL PDG 5.4.4
Figure 5-13. DisplayPort*
Auxiliary Channel Dual Mode Support Protection Circuit



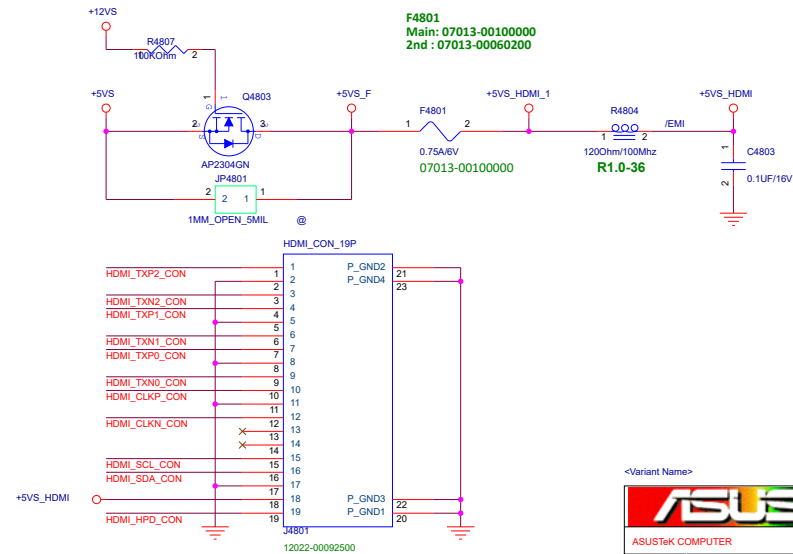
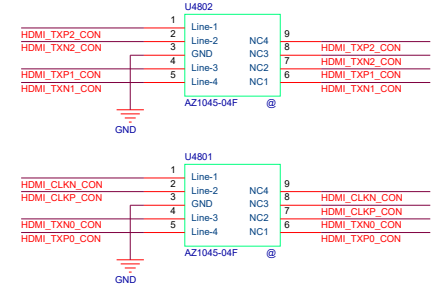
[illegible]

Figure 10 is a detailed schematic diagram of the USB PHY. It shows the internal components and connections for both USB2 and USB3. The diagram includes the following elements:

- USB2 and USB3 Inputs:** On the left, there are two pairs of input lines labeled `U3_L0R0N2`, `U3_L0R0P2`, `U3_L0T0N2`, `U3_L0T0P2` and `U3_L0R0N3`, `U3_L0R0P3`, `U3_L0T0N3`, `U3_L0T0P3`. These are connected to the `USB2` and `USB3` blocks.
- USB2 and USB3 Blocks:** The `USB2` block contains a `USB2_PHY` and a `USB2_PHY` block. The `USB3` block contains a `USB3_PHY` and a `USB3_PHY` block. These blocks are connected to the `USB2` and `USB3` ports.
- Resistors and Capacitors:** Various resistors (e.g., `R4921`, `R4922`, `R4923`, `R4924`) and capacitors (e.g., `C4905`, `C4906`) are used for signal conditioning and termination.
- Inductors:** Inductors are used for impedance matching and filtering, with values like `0.1uF/10V` and `0.1uF/10V`.
- Signal Paths:** The diagram shows the signal paths for `USB_C_U3B_N0N_X1`, `USB_C_U3B_N0P_X1`, `USB_C_U3B_P0N_X1`, and `USB_C_U3B_P0P_X1`.
- Other Components:** Other components include `U3B05A`, `U3B05B`, `U3B05C`, and `U3B05D`, which are likely part of the USB PHY's internal logic or control.

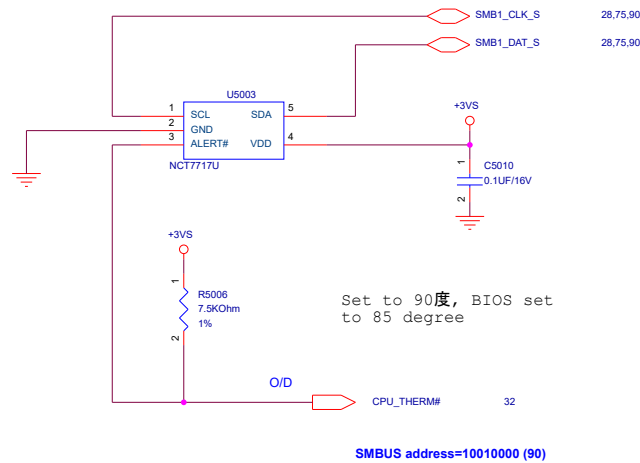
Figure 10 is a schematic diagram of the USB3.0 PHY. It shows the internal components and connections of the USB3.0 PHY. The diagram is divided into two main sections: the USB3.0_TX section and the USB3.0_RX section. The USB3.0_TX section shows the USB3.0_TXN and USB3.0_TXP pins connected to the USB3.0_TX block. The USB3.0_RX section shows the USB3.0_RXN and USB3.0_RXP pins connected to the USB3.0_RX block. The diagram also shows the internal components of the USB3.0 PHY, including the USB3.0_TXN and USB3.0_TXP pins, the USB3.0_RXN and USB3.0_RXP pins, and the USB3.0_TX and USB3.0_RX blocks. The diagram is a detailed schematic showing the internal components and connections of the USB3.0 PHY.

The schematic diagram illustrates the USB to RS-485 interface circuit. It features two USB-to-RS-485 modules, U1B03 (MAX485) and U1B04 (MAX485), connected to a common RS-485 bus. The USB side of each module is connected to +5V_B, -5V_B, D+, D-, D+, and D- pins. The RS-485 side is connected to A, B, and GND pins. The modules are connected to a common RS-485 bus via their A and B pins. The bus is terminated at both ends with 120-ohm resistors. The modules are also connected to a common RS-485 bus via their A and B pins.

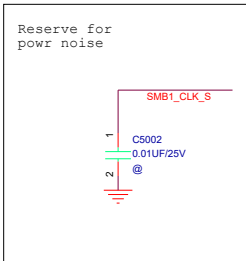
[illegible]

The diagram shows a power supply circuit for the R1.0-30 and R2.0-04 components. A +3V_CC input is connected to a network of resistors and capacitors. The network includes R4952 (100k), R4951 (100k), and two capacitors: nba_r0605_004 (0.001uF) and nba_r0605_000a (0.001uF). The output of this network is 3V. A 3VSUS input is also connected to the same network. The output of the 3VSUS input is 3VSUS.

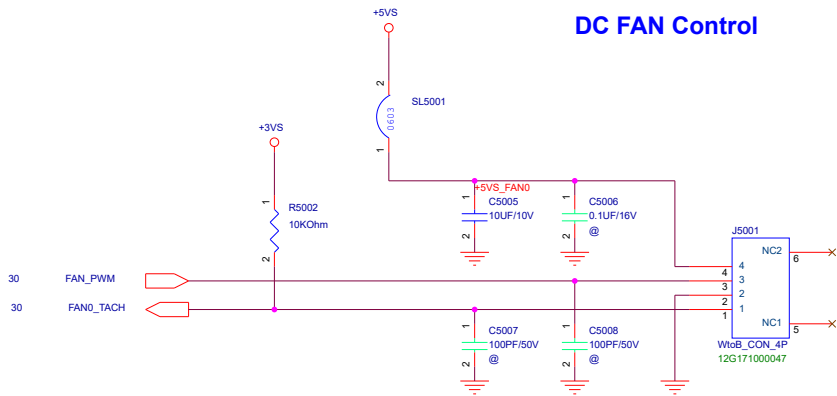
CPU Thermal Sensor



Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm



DC FAN Control



Title : FAN_Thermal Sensor & Fan

ASUSTek COMPUTER

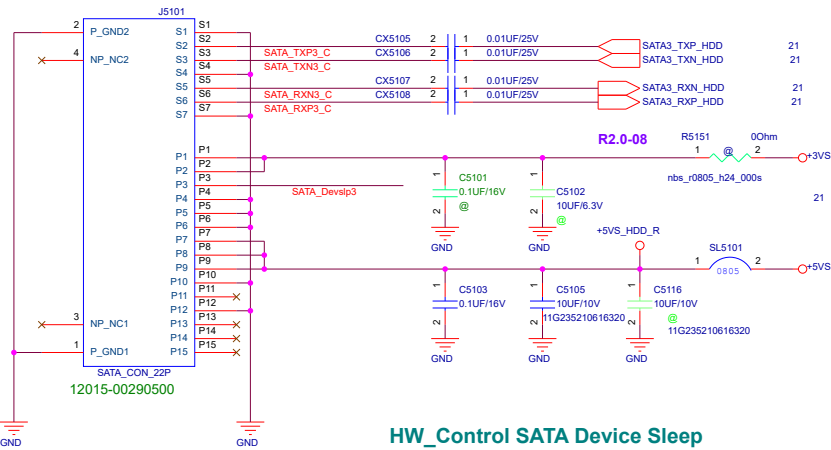
Engineer: Wendell_Lo

Size
B

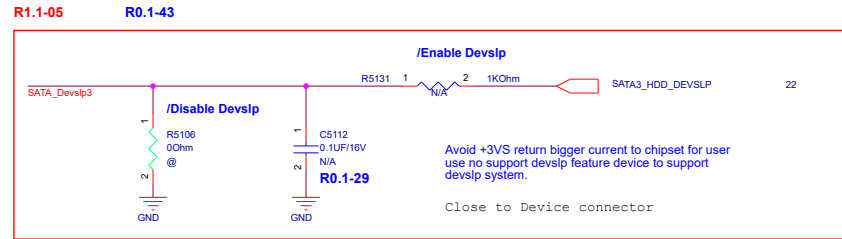
Project Name
GL752VW

Rev
1.0

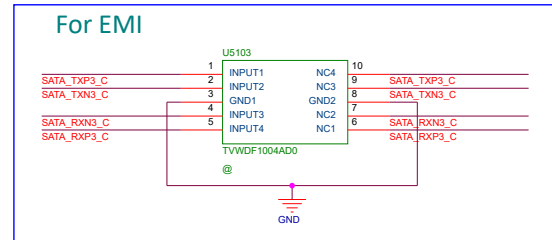
Main HDD



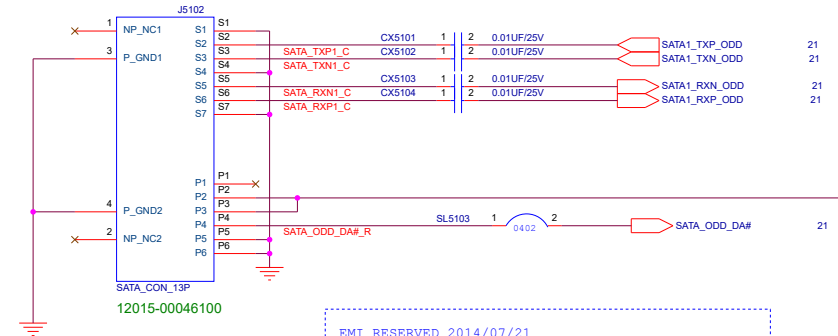
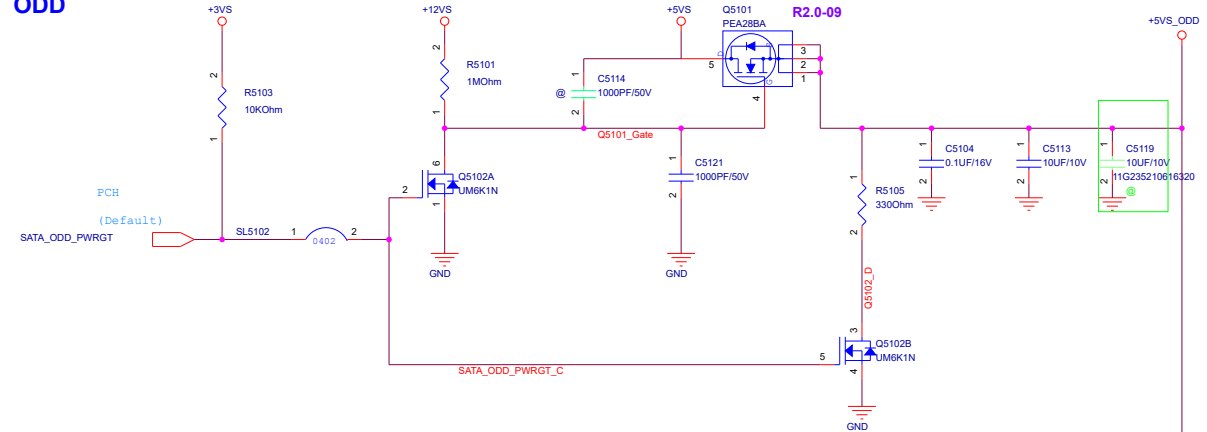
HW_Control SATA Device Sleep



For EMI



ODD



EMI RESERVED 2014/07/21

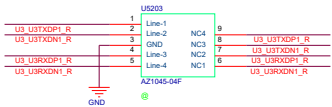
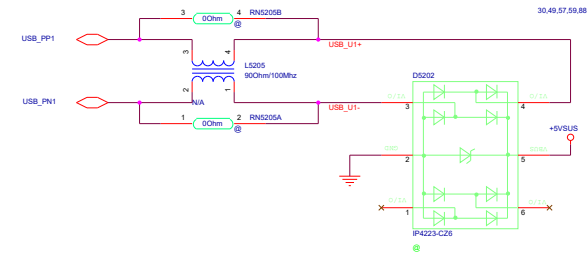


USB3.0
EMI-Protection

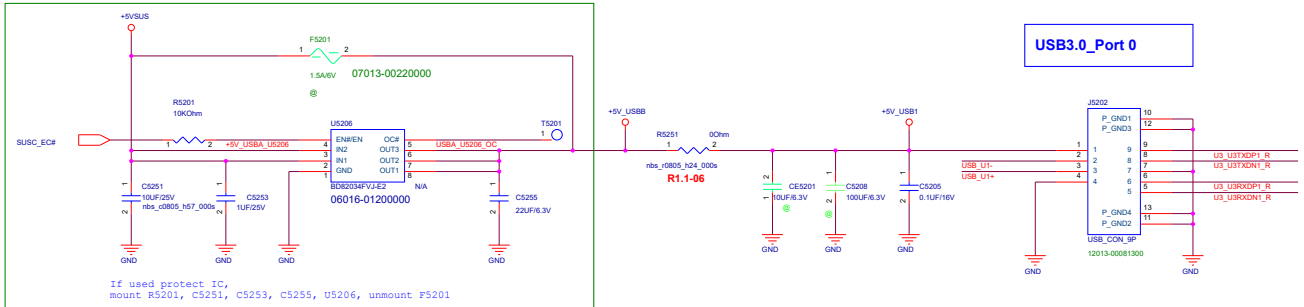
12/10/25
LS201, LS202, LS203, LS204
09G0932090400



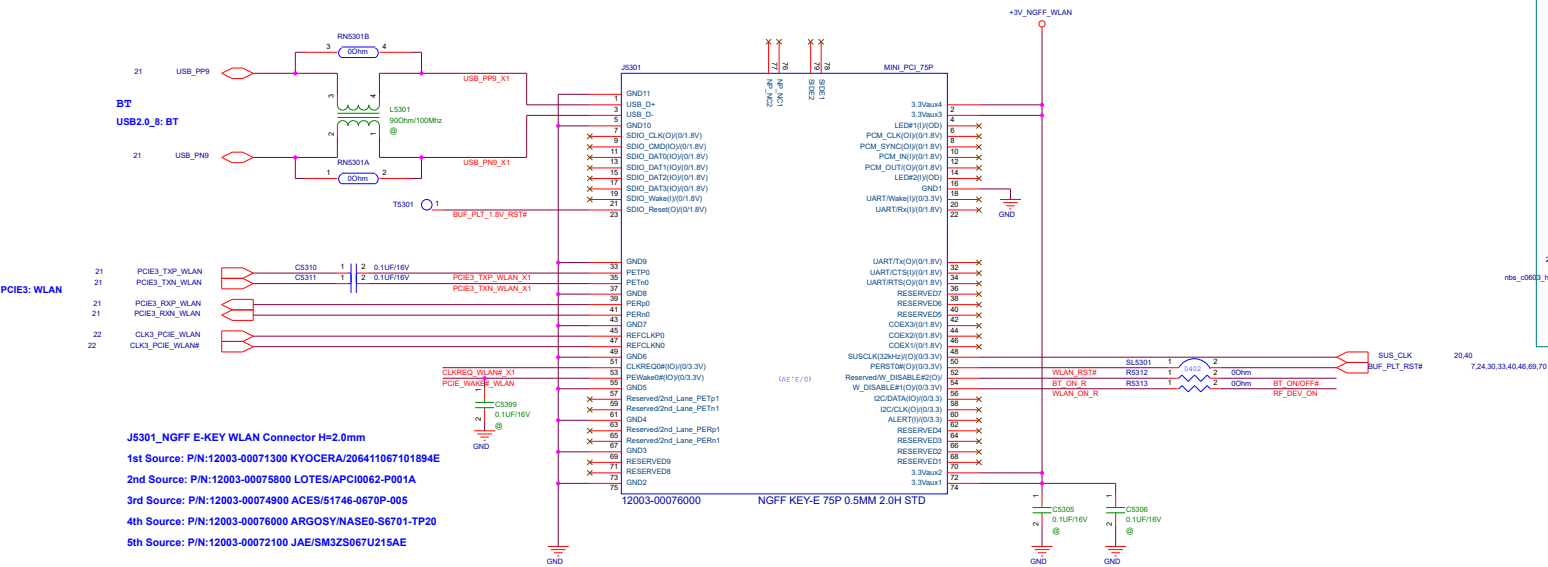
USB2.0 EMI-Protection



R1.0-14 R1.0-28



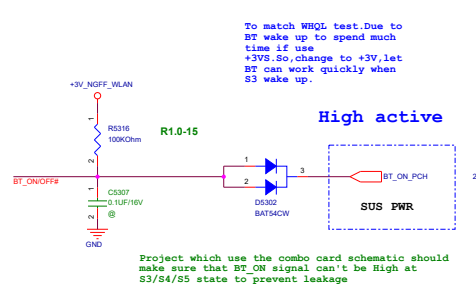
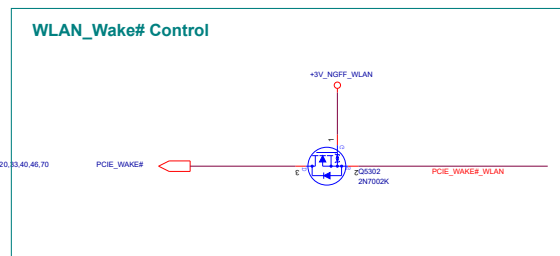
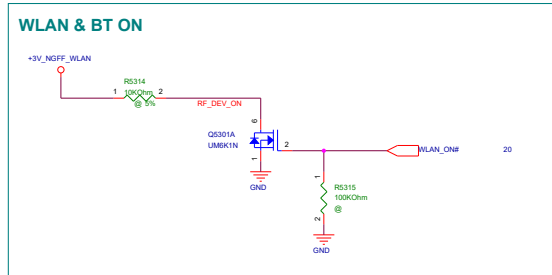
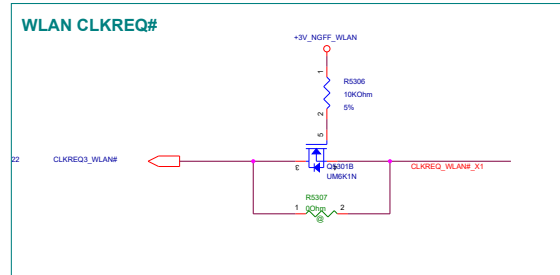
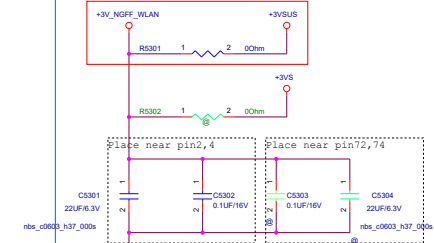
NGFF M.2 TYPE E-KEY WIFI



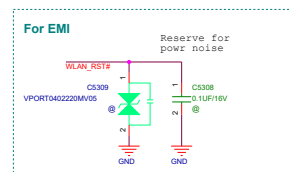
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

WLAN PWR to +3VSUS



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage



74	3-Straps	GND	75
72	3-Straps	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PETn1	67
64	GPIO NFC Reset# (MSP07)(O)(0/3,V)	Reserved/2nd Lane PETp1	65
62	NFC IC2 IRQ (MSP05)(I)(0/3,I)	GND	61
60	NFC IC2 SM CLK (IO)(0/3,I)	Reserved/2nd Lane PETn1	60
58	NFC IC2 SM DATA (IO)(0/3,I)	Reserved/2nd Lane PETp1	59
56	W_DISABLE# (O)(0/3,V)	PEWakem#(IO)(0/3,V)	55
54	Reserved/W_DISABLE#2 (O)(0/3,V)	CLKREQM (IO)(0/3,V)	53
52	PETSTOR (O)(0/3,V)	GND	51
50	SUSCLK(32KHz) (O)(0/3,V)	REFCLKIN	49
48	CODK1 (7)(0/L,V)	REFCLKP0	47
46	CODX2(7)(0/L,V)	GND	45
44	CODX1(7)(0/L,V)	PETn0	43
42	Clunk CLK	PETp0	41
40	Clunk DATA	GND	39
38	Clunk RESET (O)(0/3,V)	PETn0	37
36	UART CTS (O)(0/L,V)	PETp0	35
34	UART RTS (I)(0/L,V)	GND	33
32	UART Tx (O)(0/L,V)	Key	
		Key	
		Key	
		Key	
22	UART Rx (I)(0/L,V)	SDIO Resel(O)(0/L,V)	23
20	UART Wake (I)(0/3,V)	SDIO Wake(I)(0/L,V)	21
18	GND	SDIO DATA(O)(0/L,V)	17
16	LEDK2 (I)(OD)	SDIO DATA(O)(0/L,V)	19
14	PCM_OUT (I)(0/L,V)	SDIO DATA(O)(0/L,V)	15
12	PCM_IN (O)(0/L,V)	SDIO DATA(O)(0/L,V)	13
10	PCM_SYNC (O)(0/3,I)	SDIO CMD(O)(0/L,V)	11
8	PCM_CLK (O)(0/L,V)	SDIO CLK(O)(0/L,V)	9
6	LEDK1 (I)(OD)	GND	7
4	3-Straps	USB_D-	5
2	3-Straps	USB_D+	3
		USB_V	



Title : USB3_*****

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size

Project Name

Rev

B

GL752VW

1.0

Date: Wednesday, September 23, 2015

Sheet 54 of 102



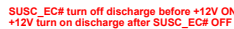
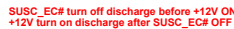
Title : **USB3_*******

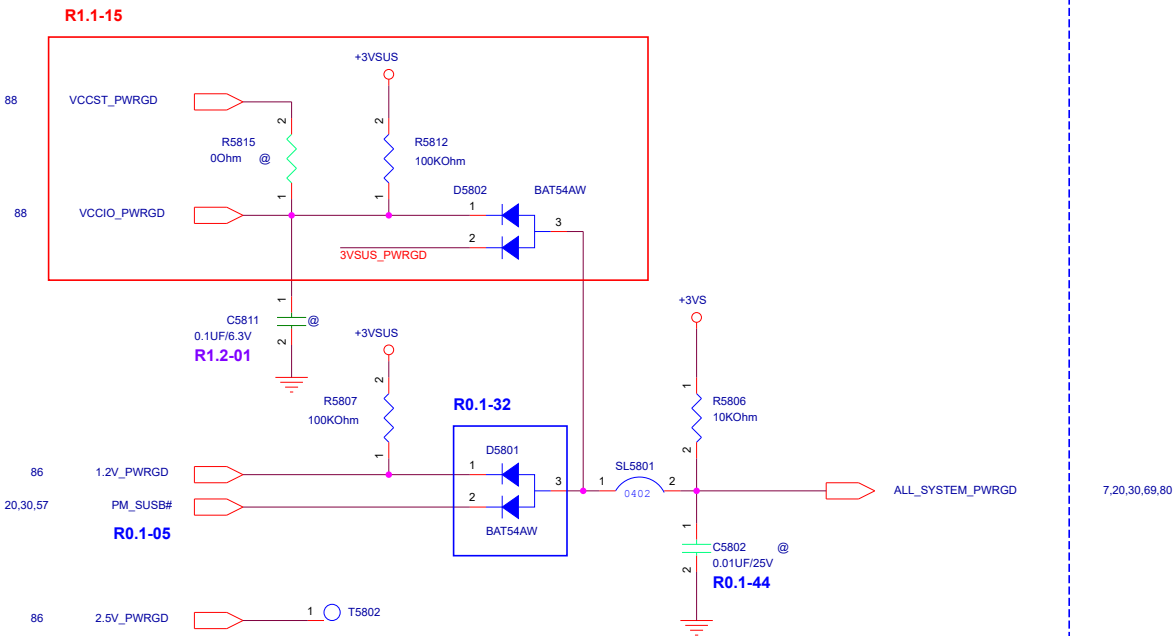
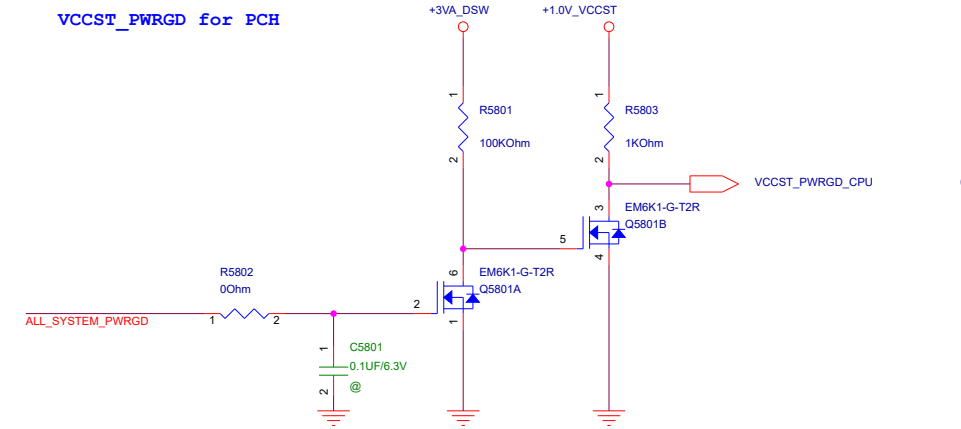
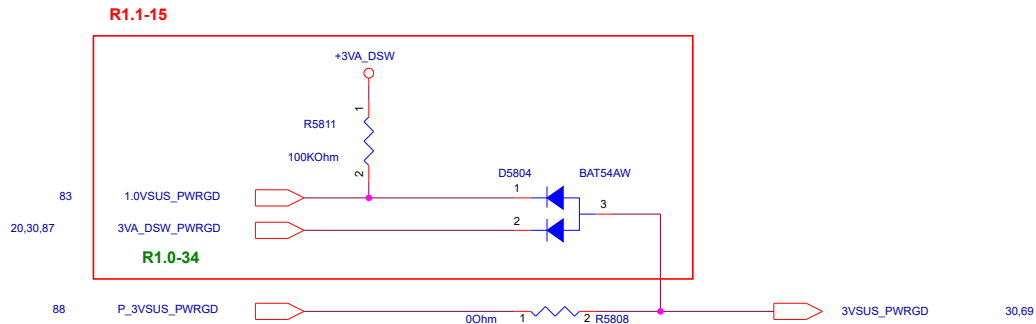
ASUSTeK COMPUTER

Engineer: **Wendell_Lo**

Size	Project Name
B	GL752VW

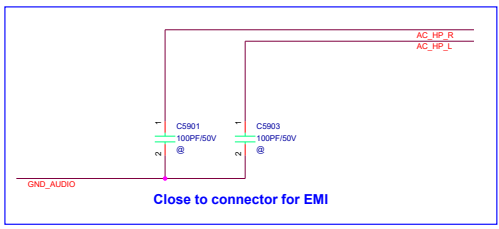
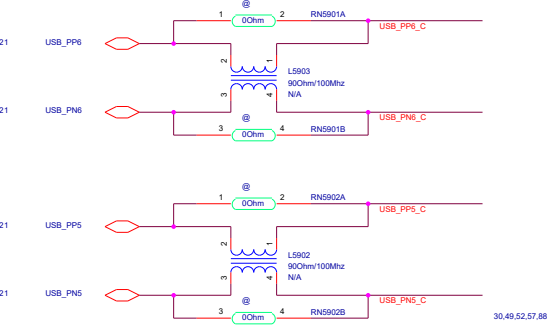
Rev
1.0



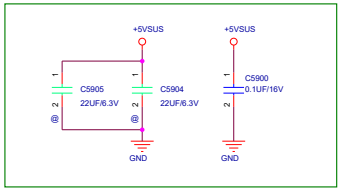


<Variant Name>

ASUS		Title : Power Protect	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	GL752VW	Rev
Custom			1.0
Date: Wednesday, September 23, 2015		Sheet	58 of 102



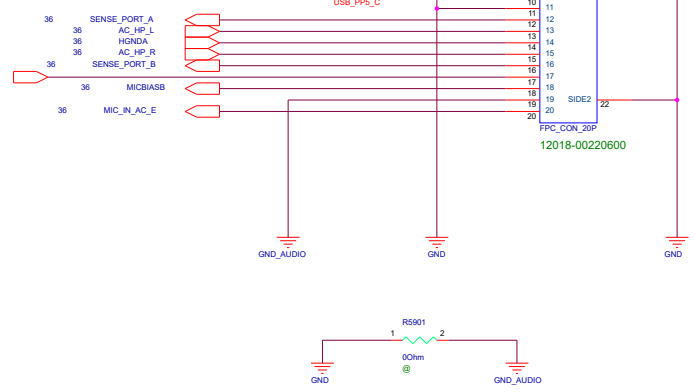
R1.0-28



To I/O Board

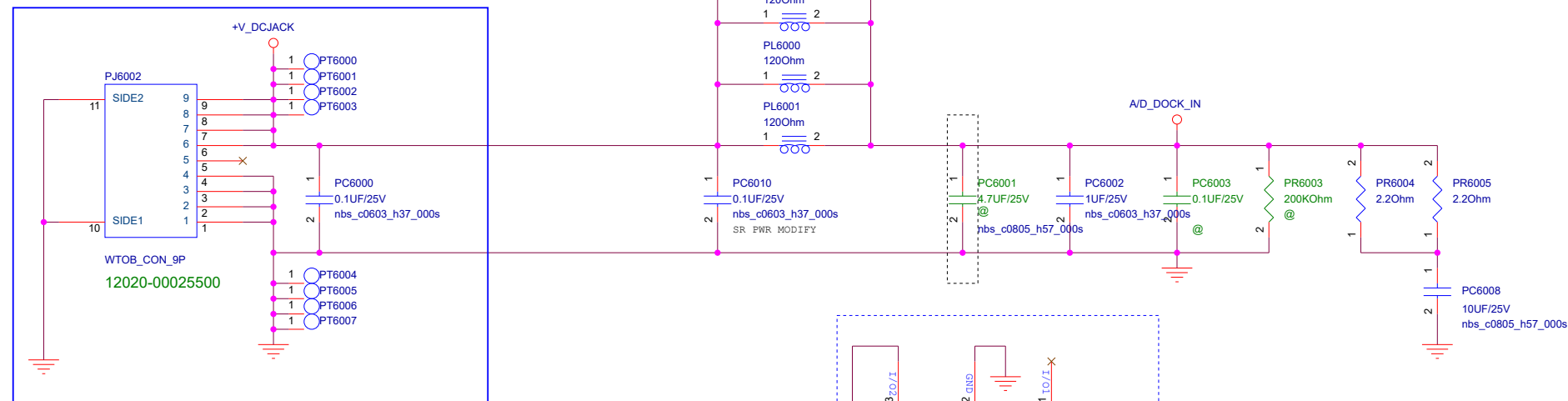
R1.0-28

SUSC_EC#

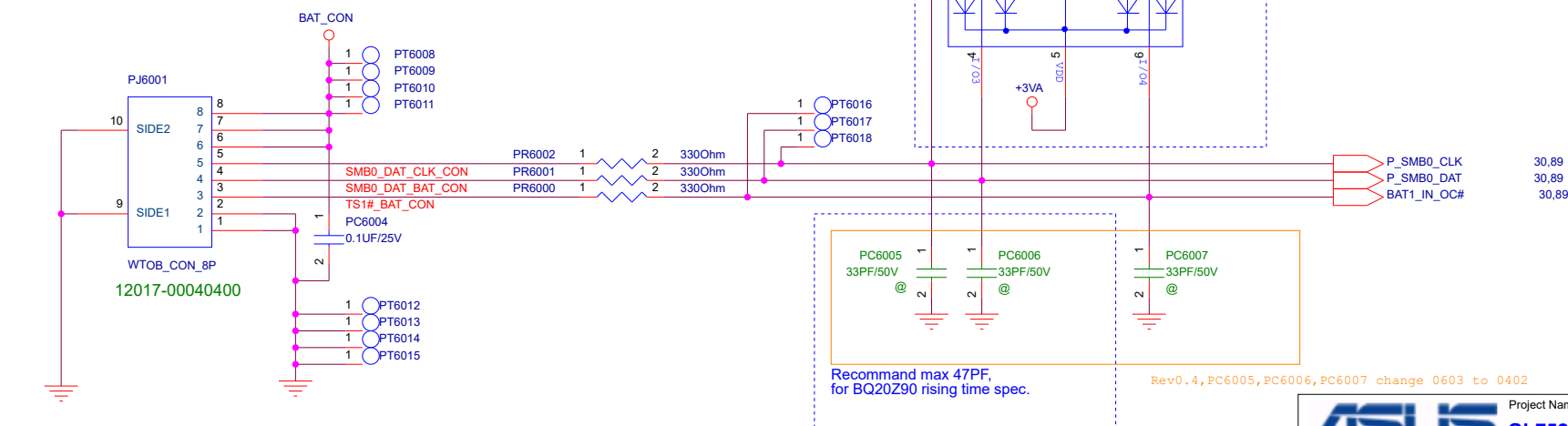


DC-IN Connector

R0.1-15

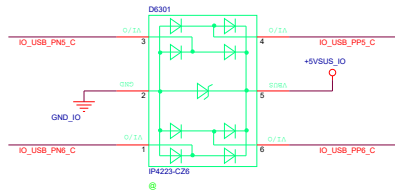
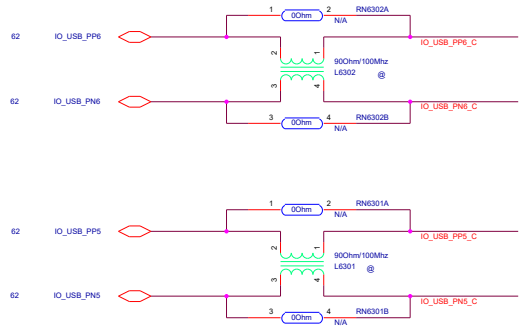
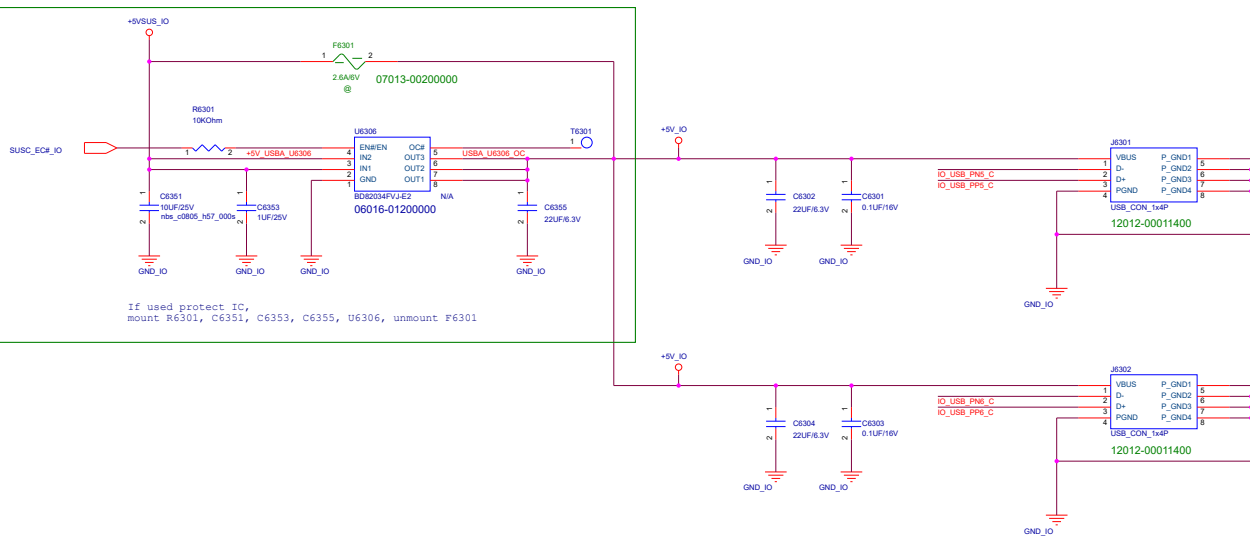


Battery Connector

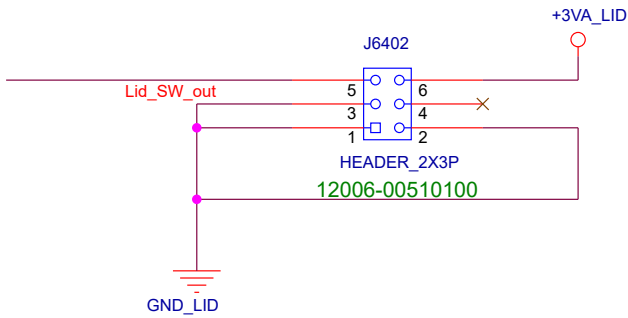
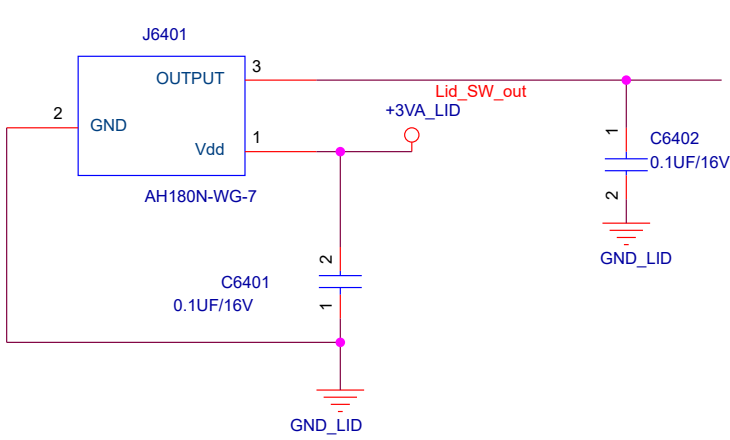


081111 -> 090604:
1. Change PD6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

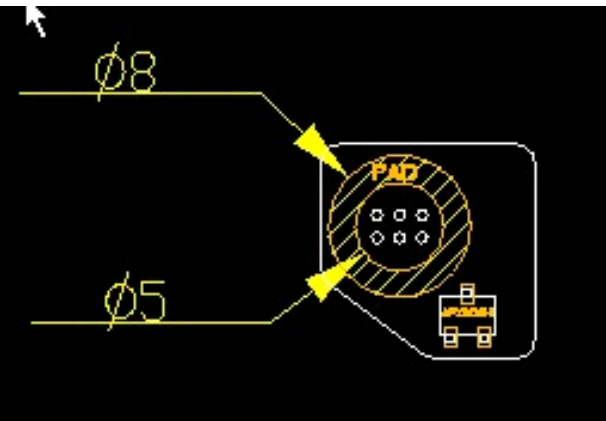
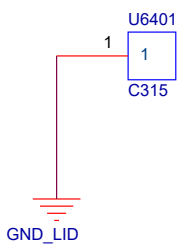
ASUS		Project Name	Rev
GL752VW			1.0
Title : DC & BAT IN			
Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo	
Date: Wednesday, September 23, 2015	Sheet	60	of 102



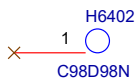
LID Switch



ME PAD



Hole



B*7

CPU

HEB15
GND
CRT27N12C36B062146

HEB17
GND
CRT27N12C36B062146

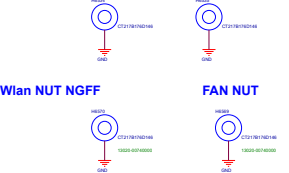
HEB16
GND
CRT27N12C36B062146

GPU

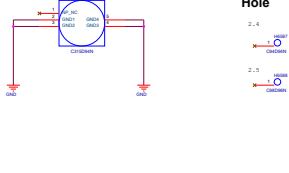
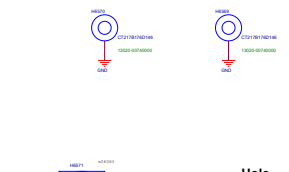
HEB16
GND
CRT27N12C36B062146

HEB17
GND
CRT27N12C36B062146

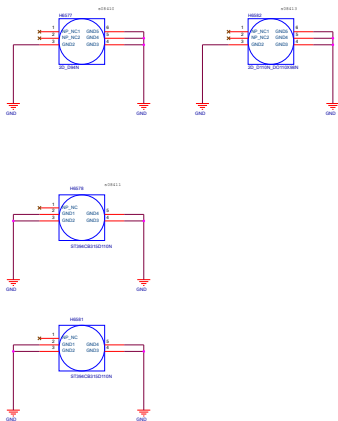
HEB15
GND
CRT27N12C36B062146



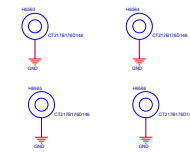
Wlan NUT



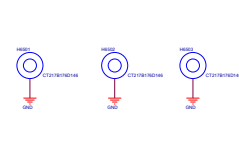
Hole



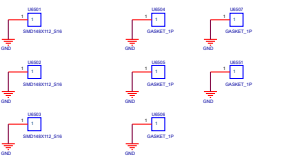
Colay CPU NUT for ME request



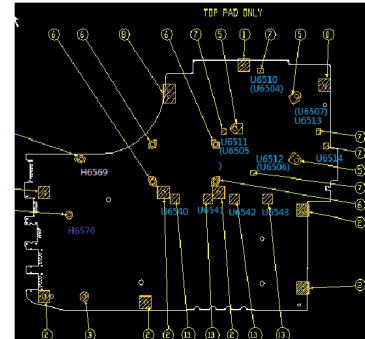
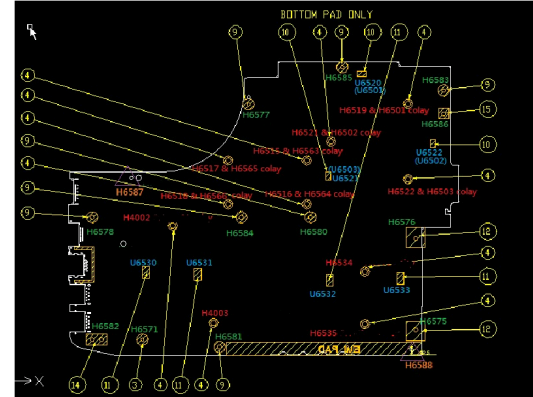
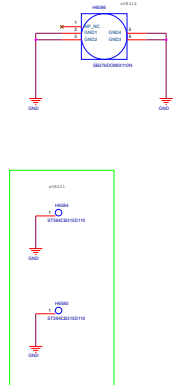
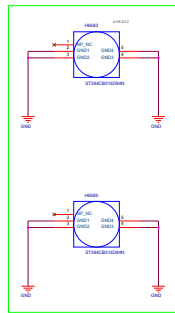
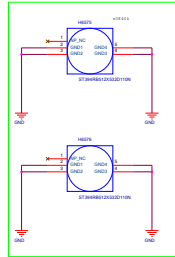
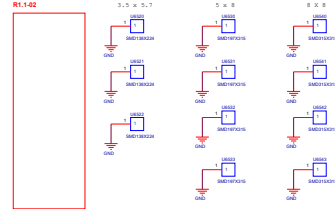
Colay GPU NUT for ME request



EMI SPRING



ME PAD



		Title : *****	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	Rev	
B	GL752VW	1.0	
Date: Wednesday, September 23, 2015		Sheet	66 of 102



Title : *****

ASUSTeK COMPUTER

Engineer: **Wendell_Lo**

Size	Project Name
B	GL752VW

Rev
1.0

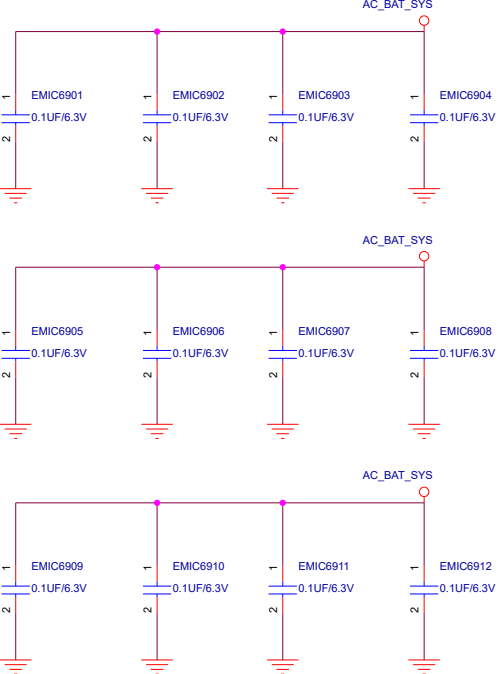


Title : OTH_for test only

ASUSTeK COMPUTER

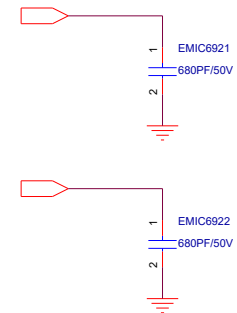
Engineer: Wendell_Lo

Size	Project Name	Rev
B	GL752VW	1.0



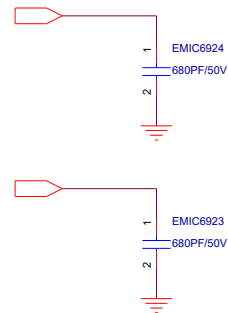
7,24,30,33,40,46,53,70

BUF_PLT_RST#



7,20,30,33

PM_RSMRST#

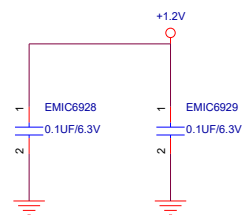


30,58

3VSUS_PWRGD

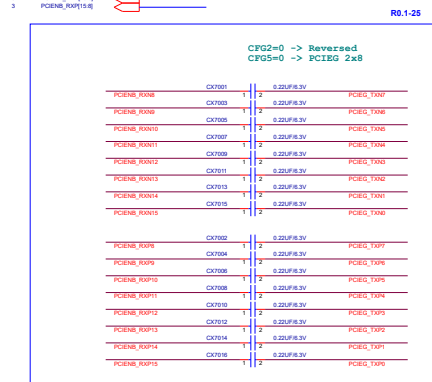
7,30,31,32

R1.0-36
PWR_SW#

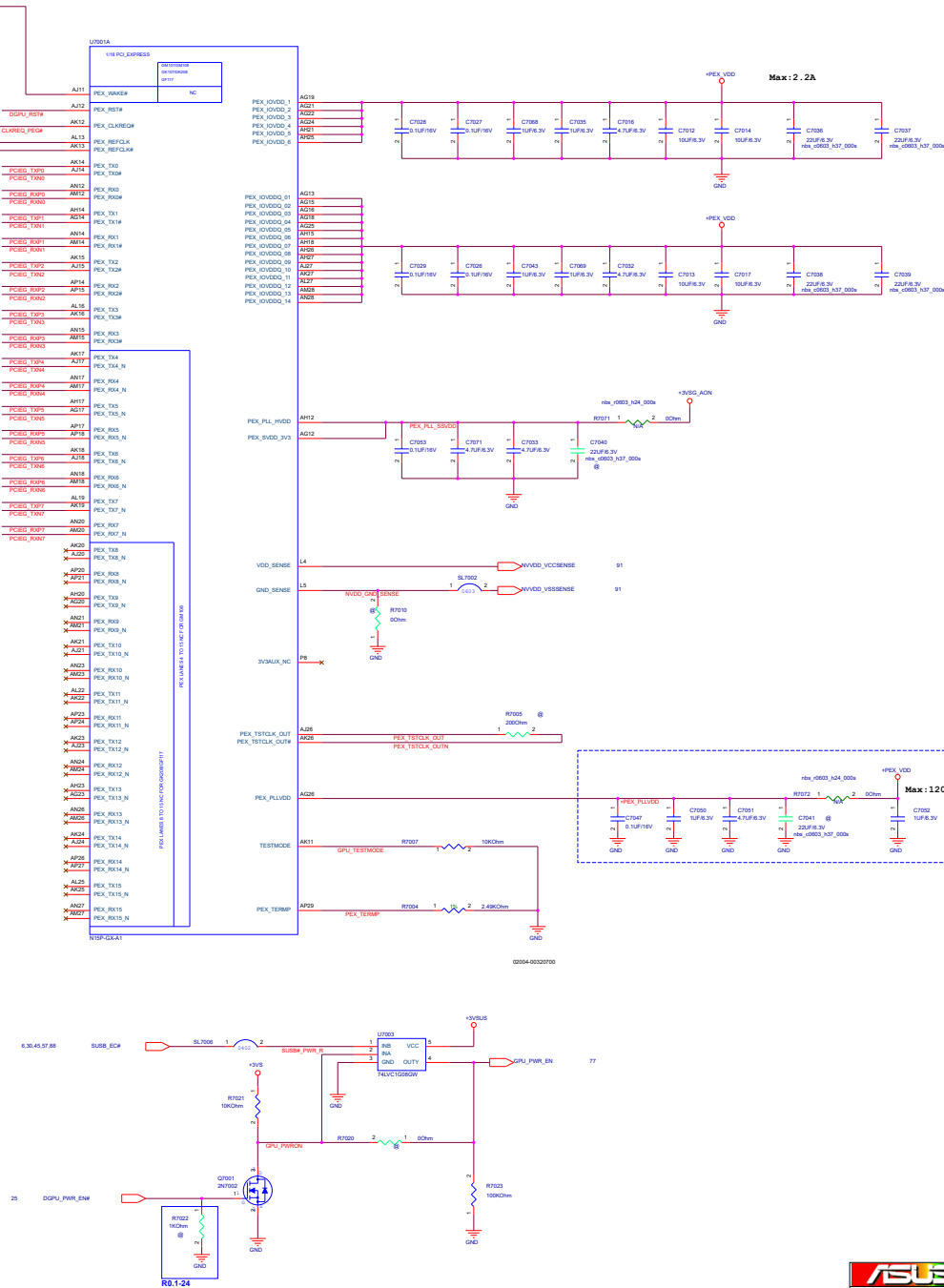
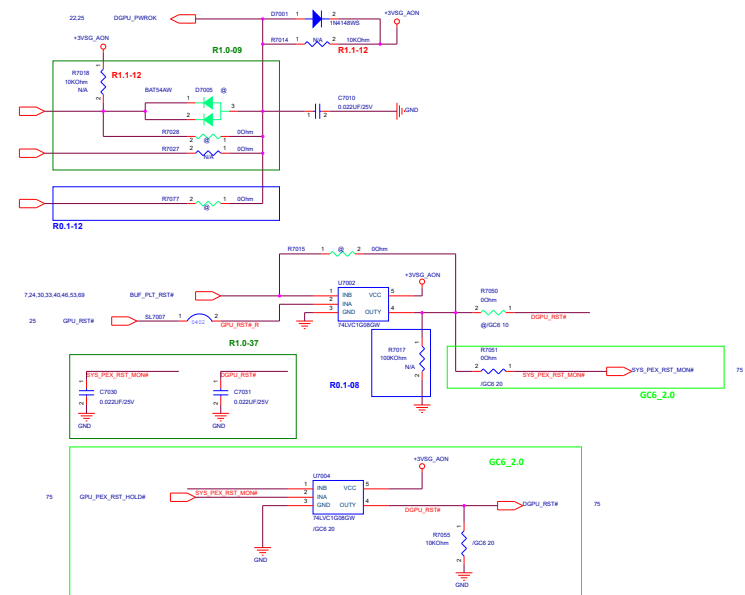


		Title : OTH_EMI Caps	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size B	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 69 of 102	

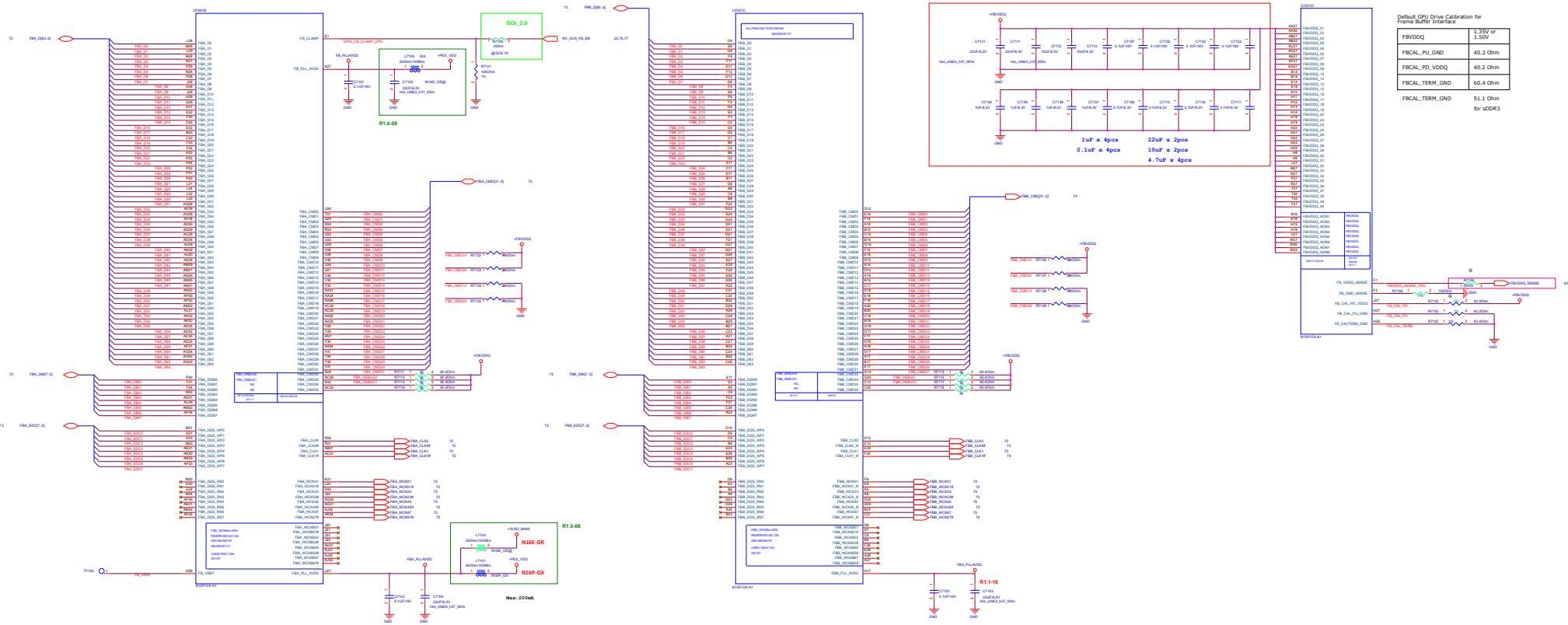
3	PCIEG_RXN[7:0]		
3	PCIEG_RXP[7:0]		
3	PCIEB_RXN[15:8]		
3	PCIEB_RXP[15:8]		



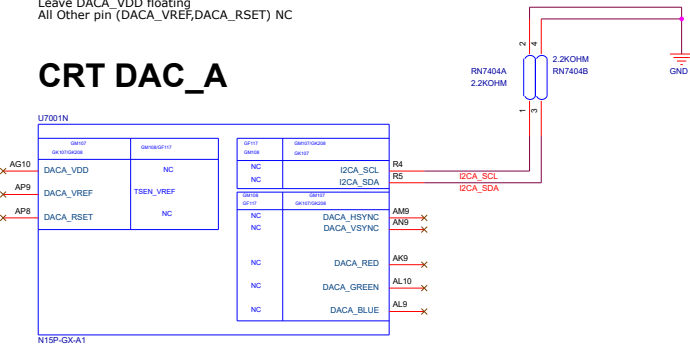
Control Signal from PCH



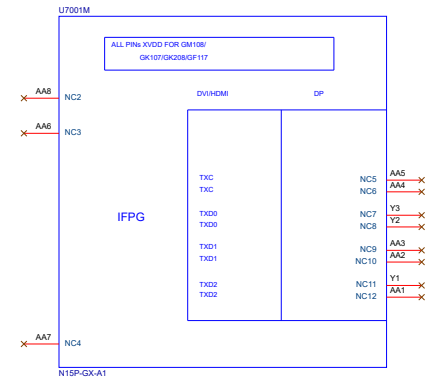
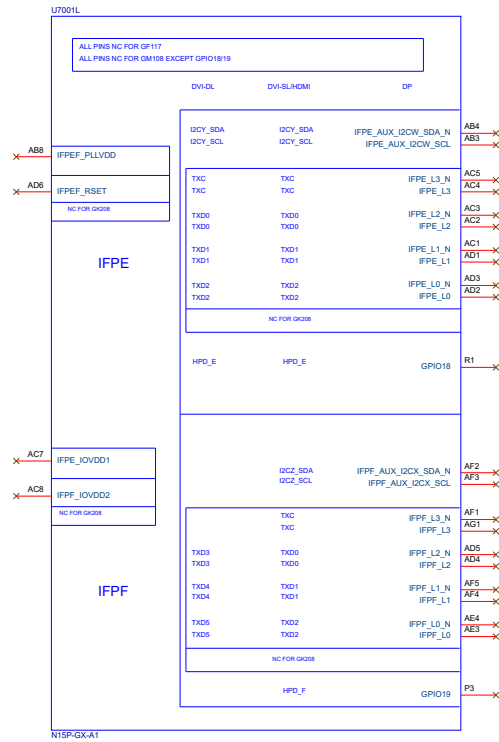
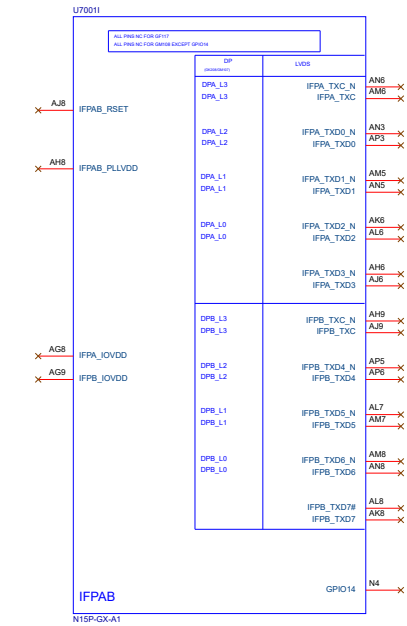
M7 Review 2014.11.12



DG-06246-001_v02 DG10.2.1 p168
Unused I2C should be soft grounded or
PU 3.3V via 2.2kOhm

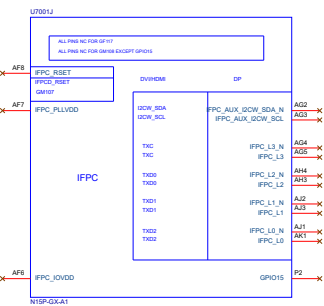


DG-06246-001_v04 DG8.6 p162
Float IFPxy_IOCDD/IFPxy_PLLVDD
Other pin NC

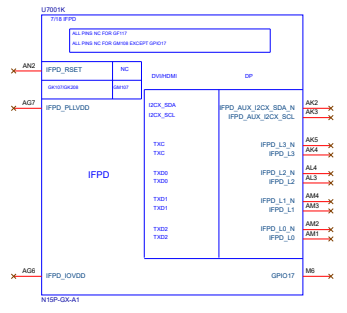


DP(link C)

DG-06246-001_v02 p157 DG8.6
 I/F not used
 IFPxy_10CDD/IFPxy_PLLVDD 10K PD
 Other pin NC



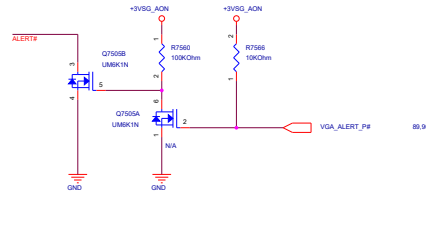
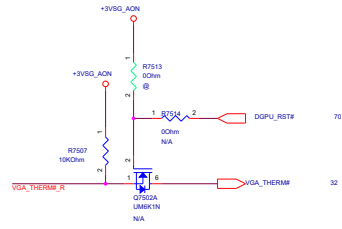
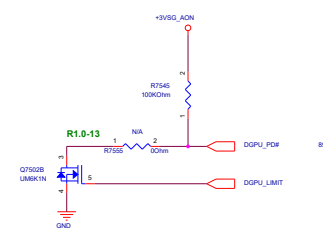
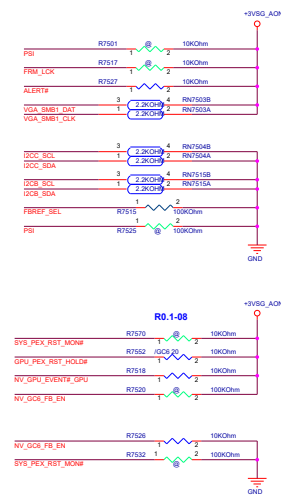
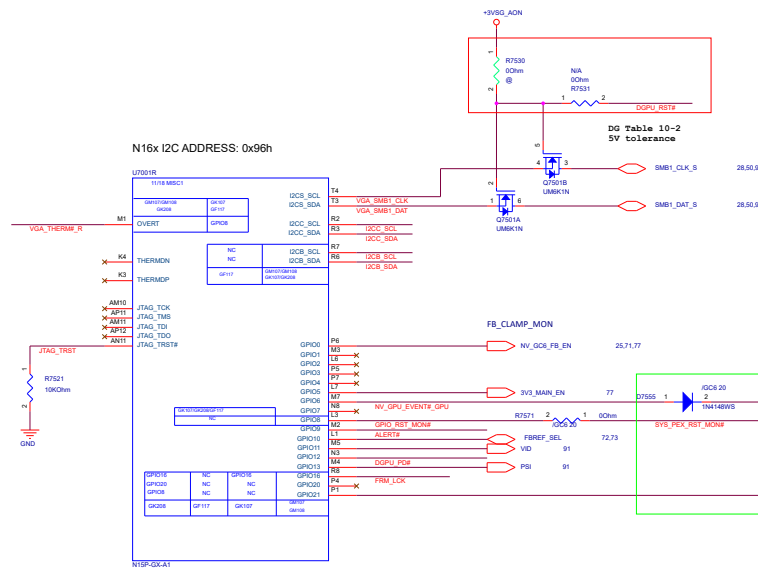
DVI(link D)

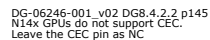


DG-07158-001_v05_secured Table 12-2.

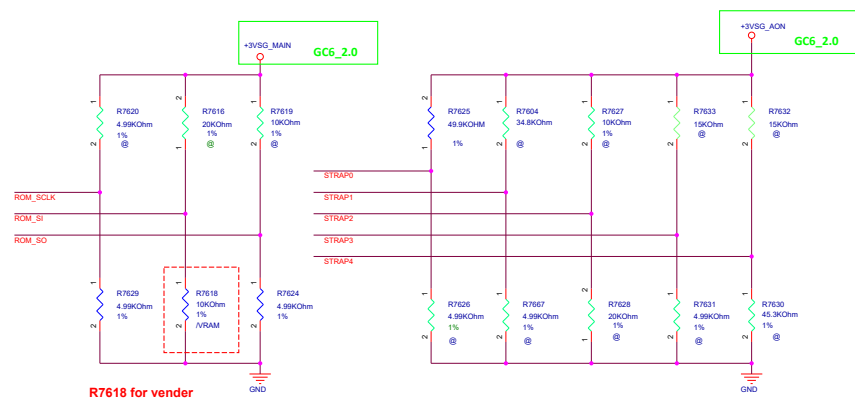
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT	Low	GC6_FBEN
1	OUT	High/Low	MEM_VDD_CTL
2	OUT	Low	LCD_BL_PWM
3	OUT	Low	LCD_VCC
4	OUT	Low	LCD_BLEN
5	OUT	High	3V3_MAIN_EN
6	IN	High	GPU_EVENT#
7	OUT	Low	3Dvision
8	IN	High	SYS_PEX_RST_MON#
9	I/O	High	THERM_ALERT
10	OUT	Low	MEM_VREF_CTL
11	OUT		PWM_VID
12	IN	High	PWM_LEVEL
13	OUT	High	PSI
14	IN	Fig. 12-1	HPD_IFPAB
15	IN	Fig. 12-1	HPD_IFPC
16	IN	High	FRAME_LOCK#
17	IN	Fig. 12-1	HPF_IPFD
18	IN	Fig. 12-1	HPD_IPFE
19	IN	Fig. 12-1	HPD_IPFFB
20			Reserved
21	OUT	High	GPU_PEX_RST_HOLD#
OVERT	I/O	High	OVERT





STRAPPING OPTIONS for N16P



USE GDDR5 VRAM 128Mb x 32 (512MB)

Hynix strap 0x6 HYNIX/H5GC4H24AJR-T2C - 34.8Kohm +1.35V

Micron strap 0x4 Micron/EDW4032BABG-60-F - 24.9Kohm +1.35V

Samsung strap 0x3 Samsung/K4G41325FC-HC04 - 20Kohm +1.5V non-RVL

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)

2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

	PU	PD
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

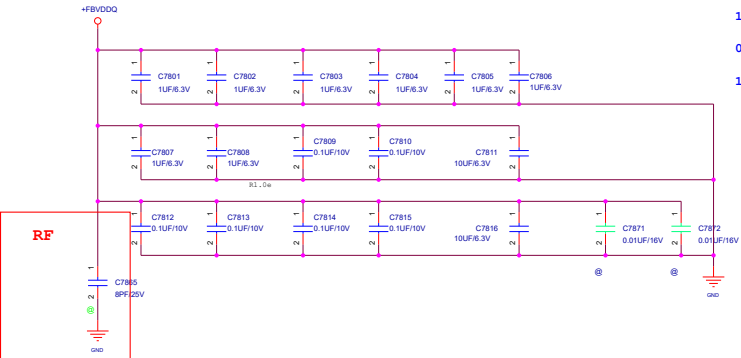
Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Do not stuff.			

Table 7. N16P-GX GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GC2H48FR-T2C	B-die	0x1	2500	1347	Production candidate
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500	N/A	Production candidate
			Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production candidate
		256Mx16	Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production candidate
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production candidate
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production candidate

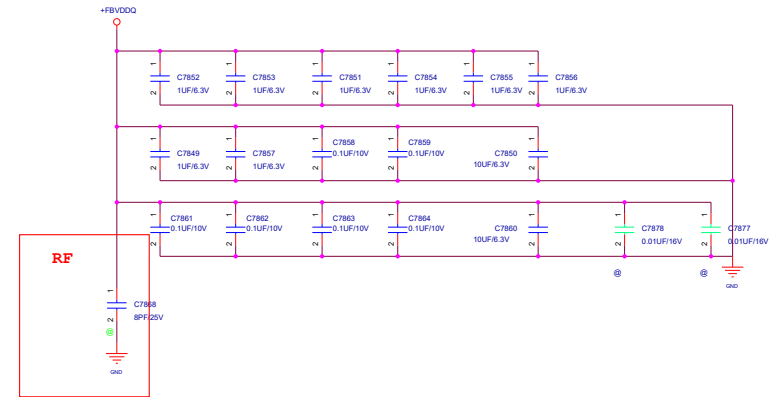
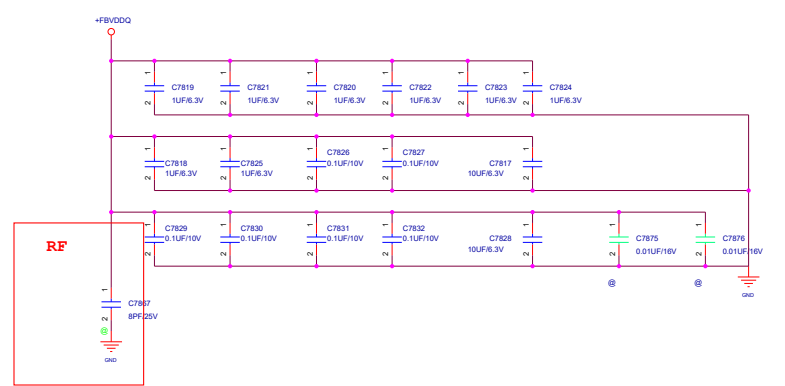
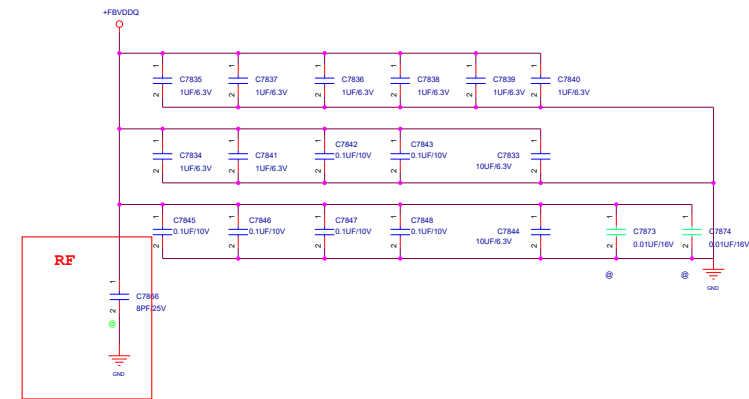
Per 1x32 or 2x16 for GDDR5 Memory



1uF x 8pcs

0.1uF x 6pcs

10uF x 2pcs





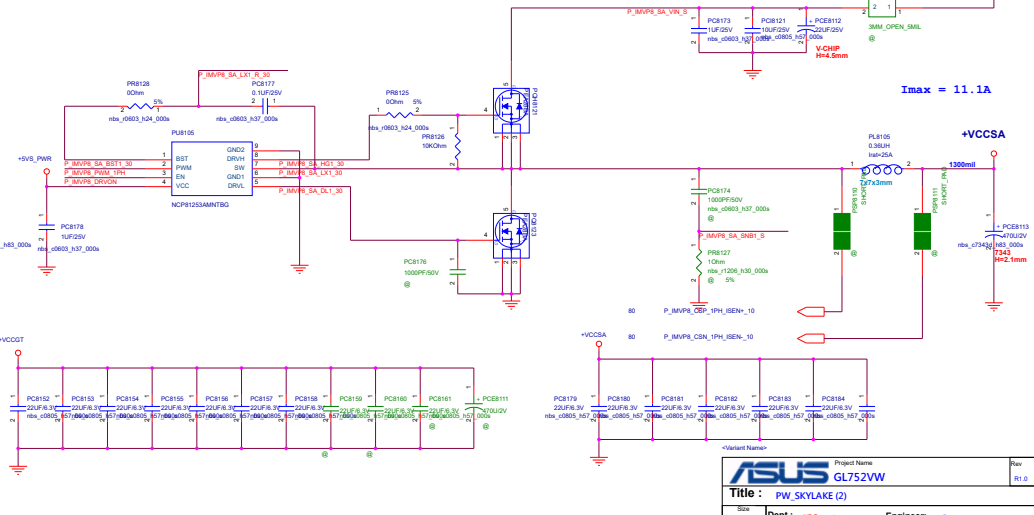
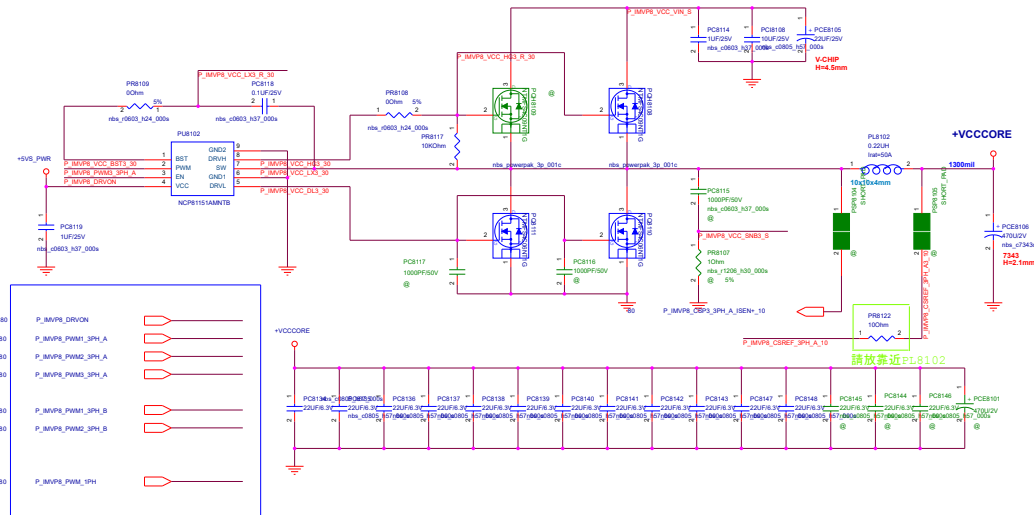
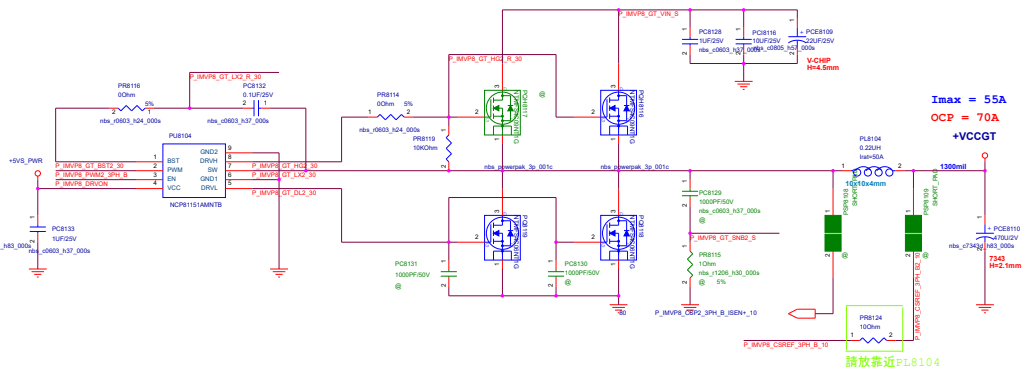
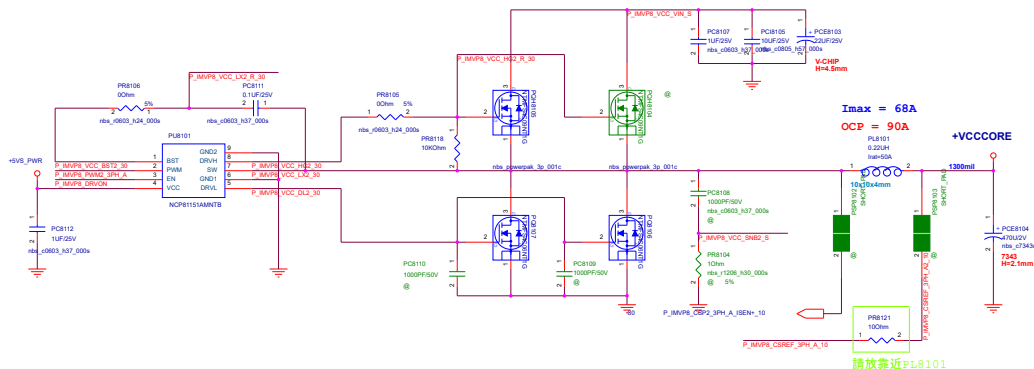
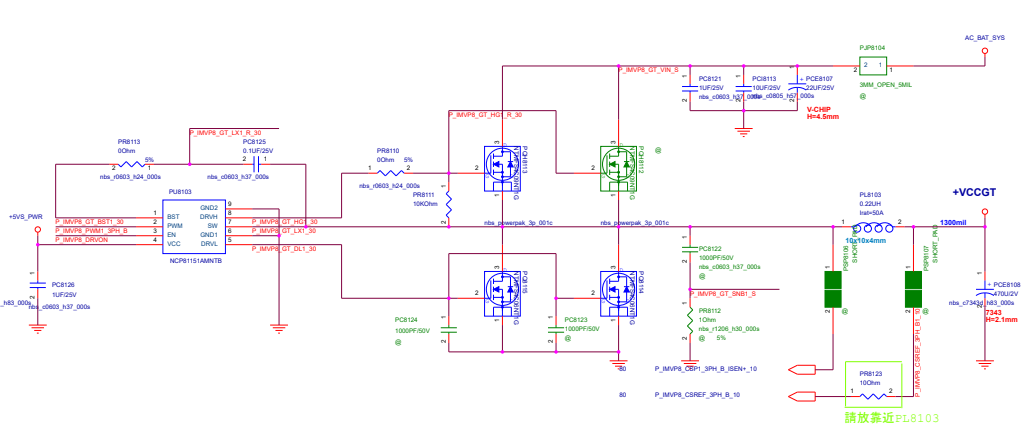
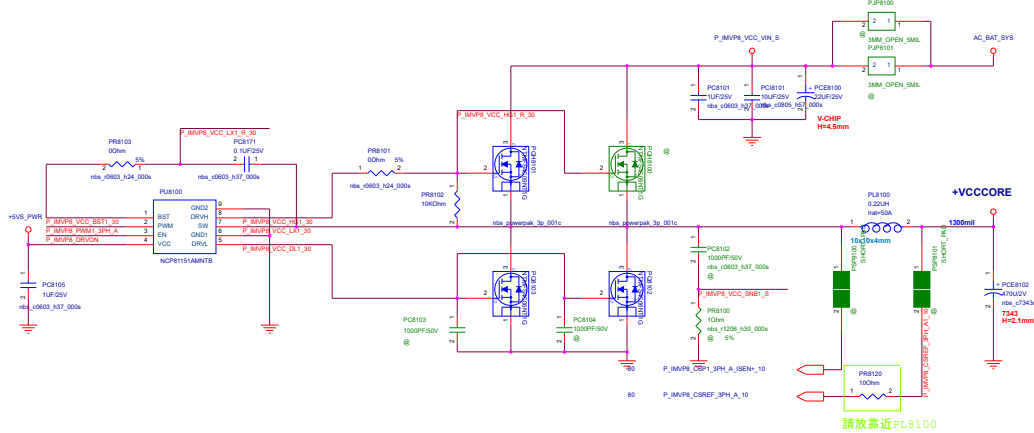
Title : SBU_DGPU_*****_R0.9

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
B	GL752VW	1.0

Skylake IMVP8 Power [For CPU]





Project Name

GL752VW

Rev

1.0

Title : PW_SKYLAKE (3)

Size

B

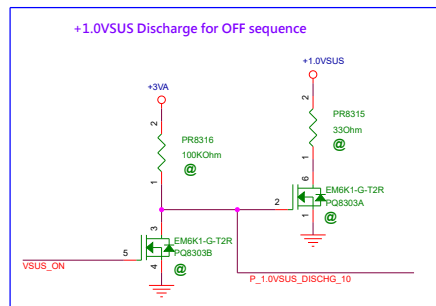
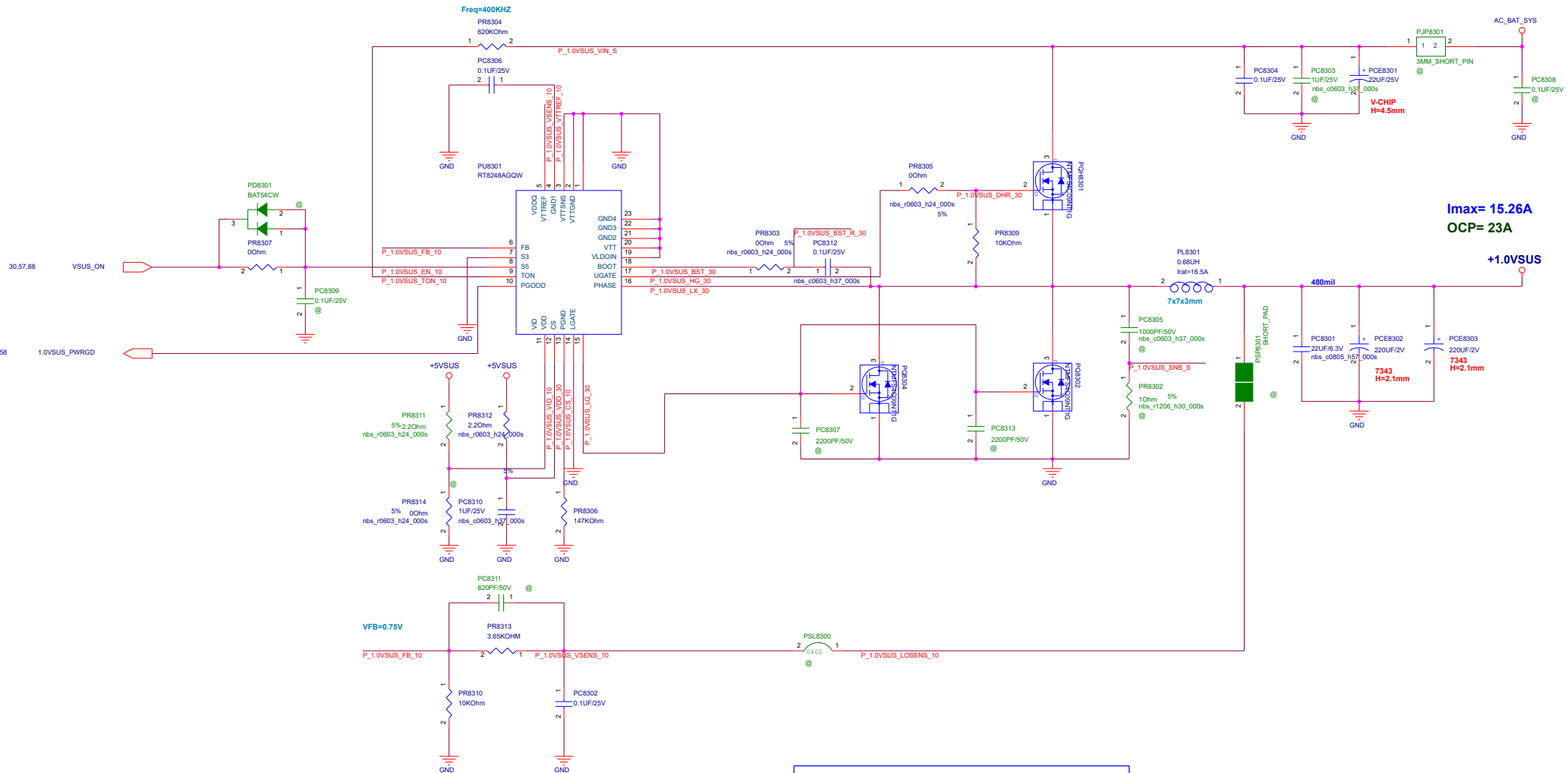
Dept.: NB Power team

Engineer: Joe

Date: Wednesday, September 23, 2015

Sheet 82 of 102

+1.0VSUS [For PCH]





Project Name

GL752VW

Rev

1.0

Title : PW_+VCCIO

Size

B

Dept.: NB Power team

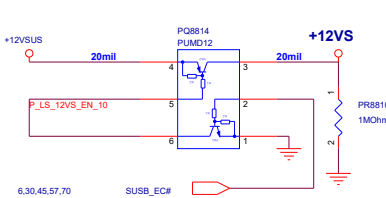
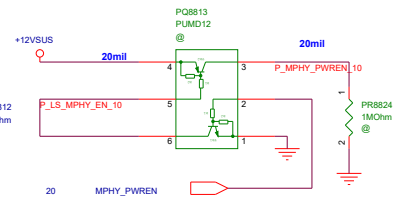
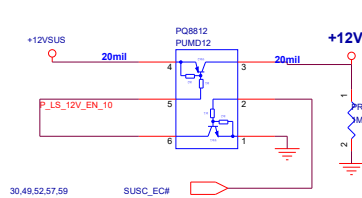
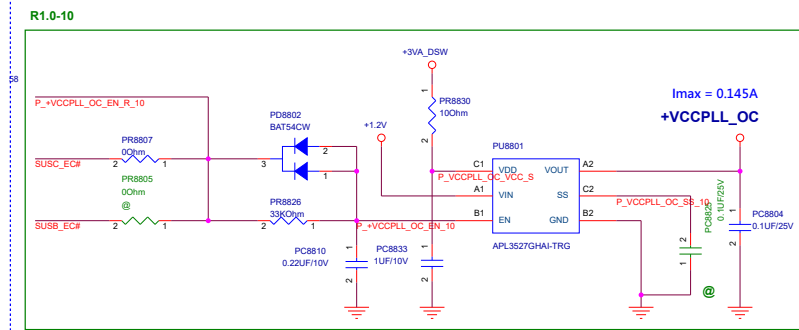
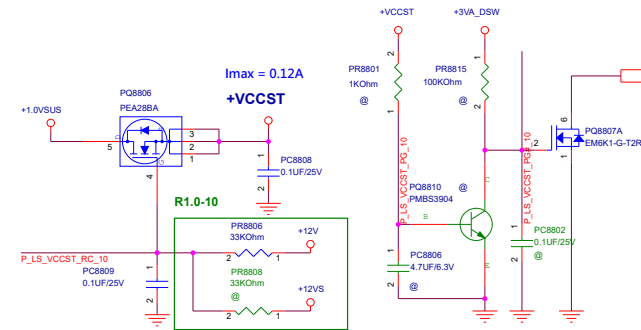
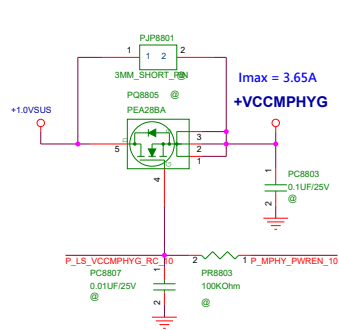
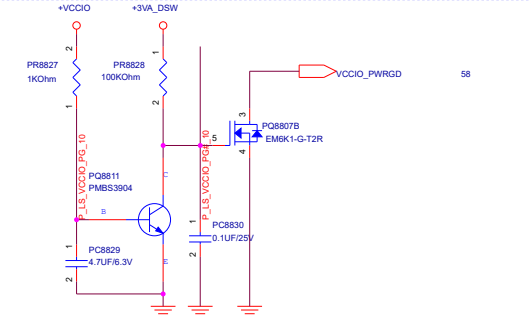
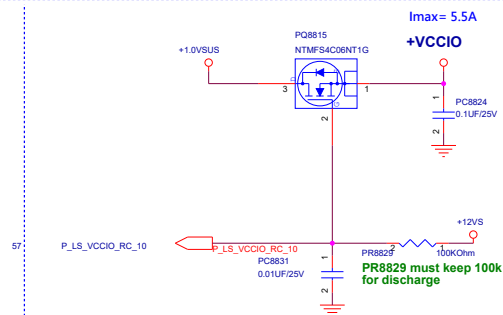
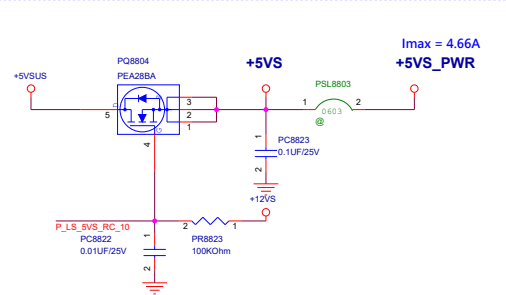
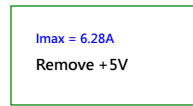
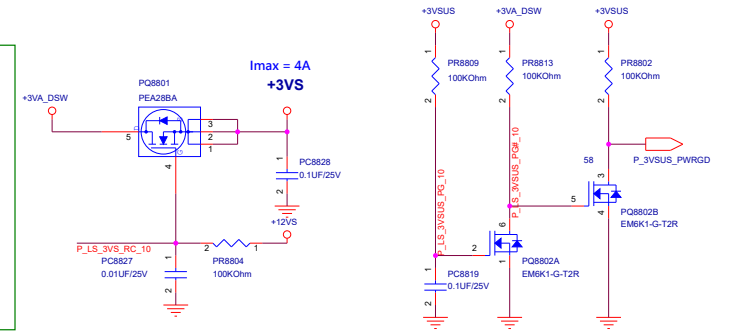
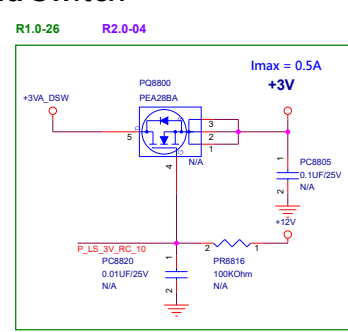
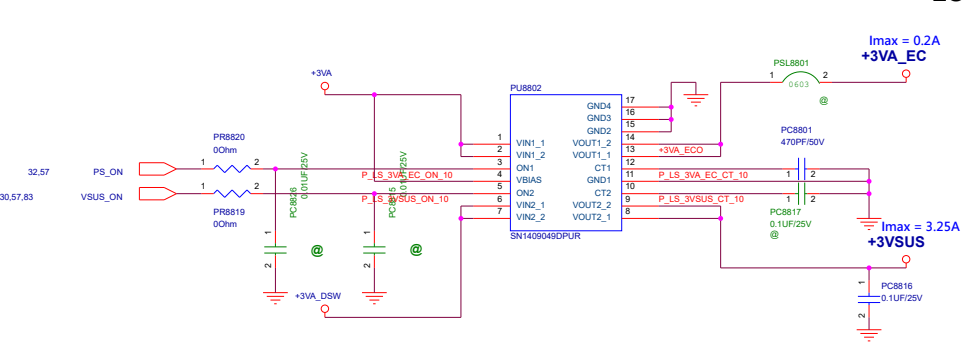
Engineer: Joe

Date: Wednesday, September 23, 2015

Sheet 84 of 102

		Project Name GL752VW		Rev 1.0
Title : POWER_VGFX_CORE				
Size B	Dept.: NB Power team		Engineer: Joe	
Date: Wednesday, September 23, 2015			Sheet	85 of 102

Load Switch



Address Selection Table

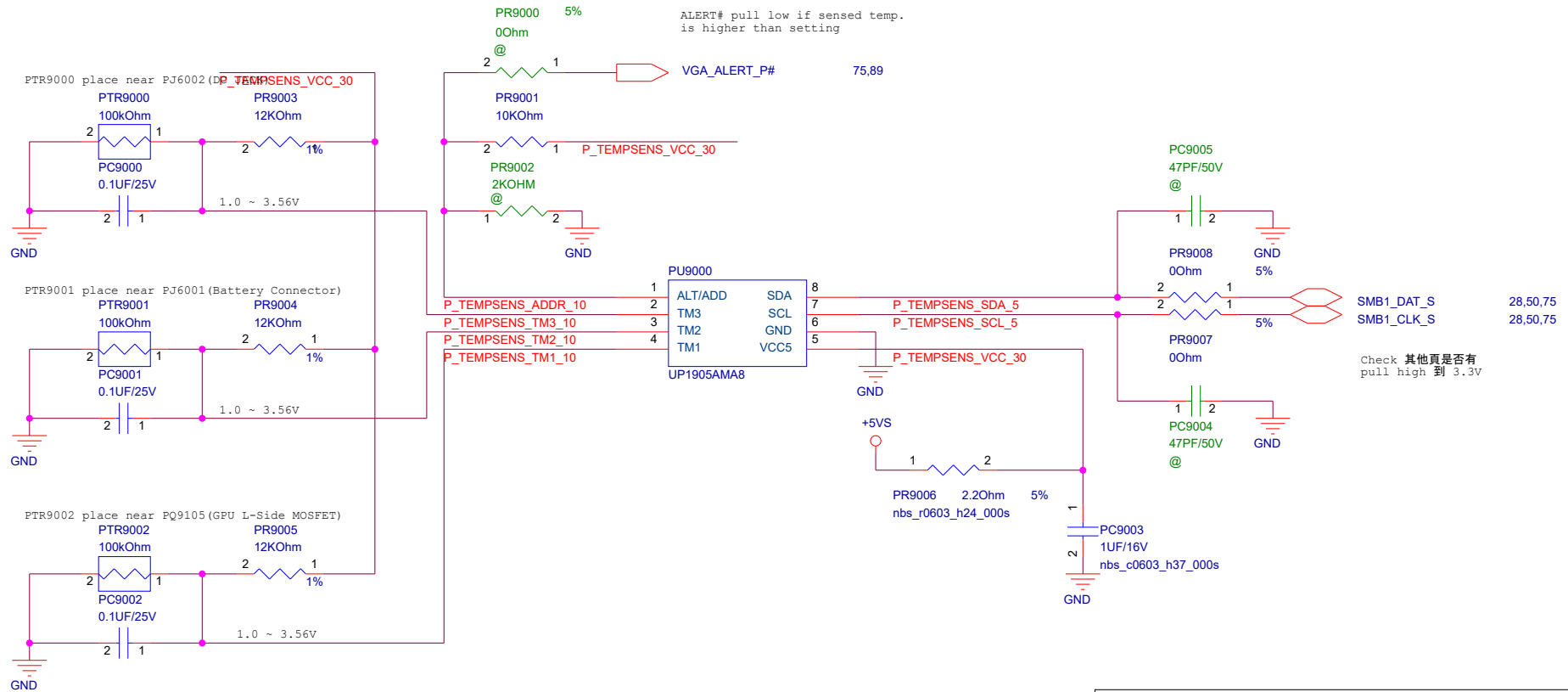
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9404	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9405	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Main 2nd

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

Main Board

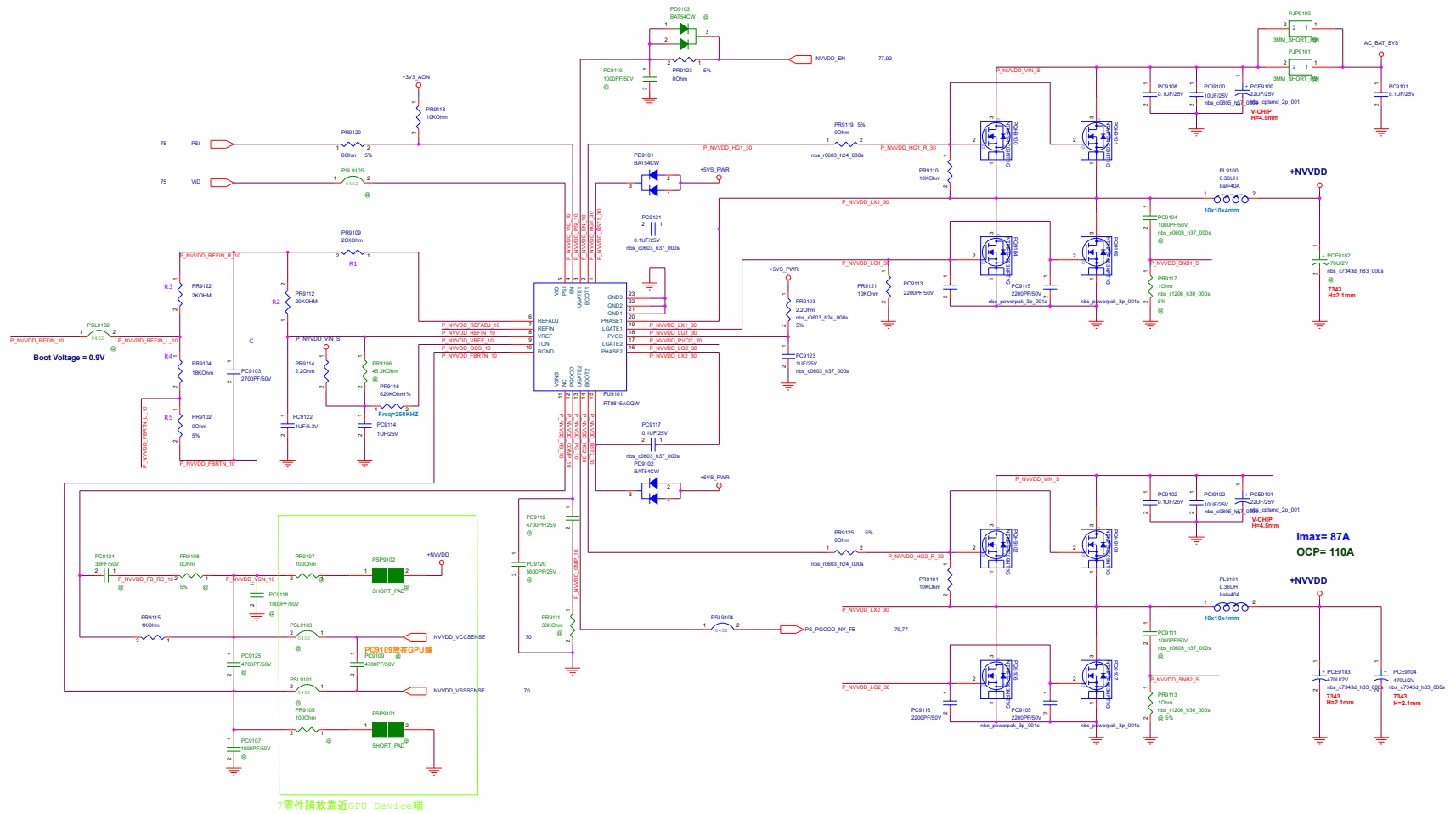


Project Name		Rev
ASUS GL752VW		1.0
Title : PW_PROTECTION		
Size	Dept.:	Engineer:
Custom	NB Power team	Joe
Date:	Wednesday, September 23, 2015	Sheet 90 of 102

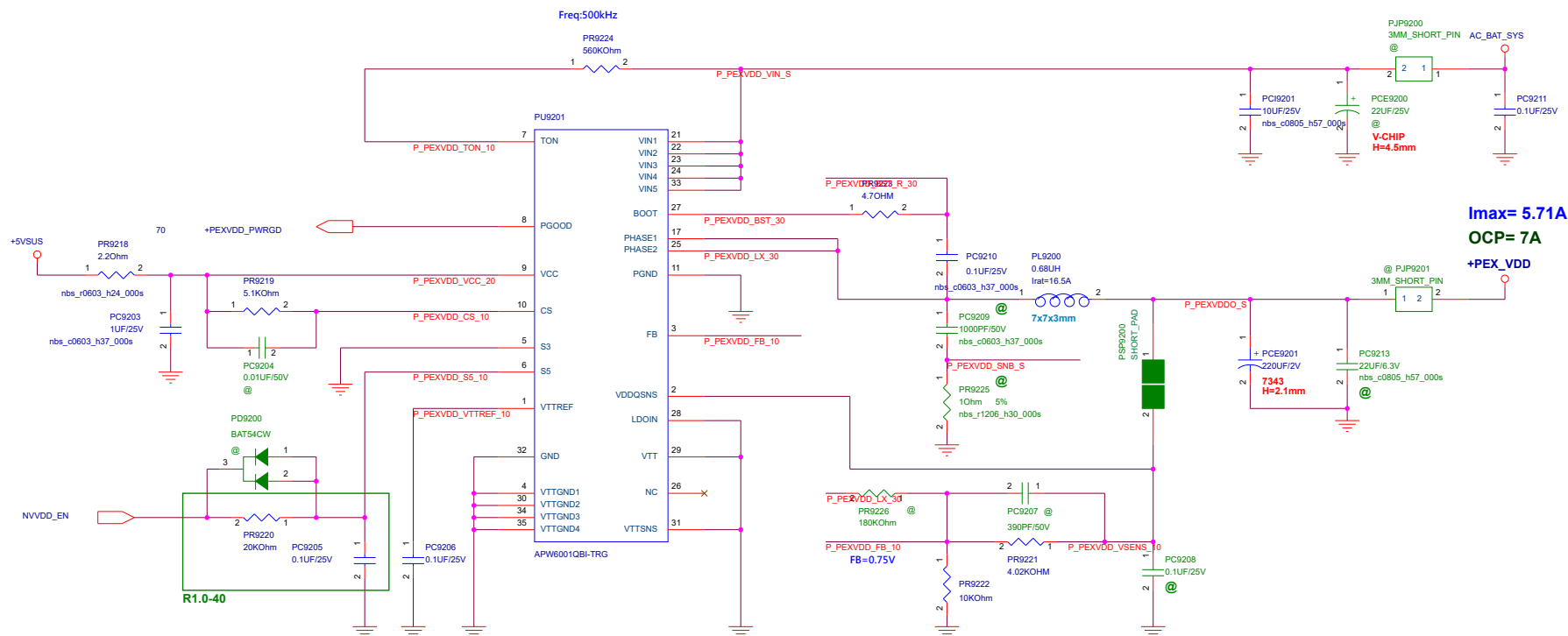
+NVVDD [For DGPU]

PWM-VID Spec

	Config A	Config B
R1 (kohn)	39	20
R2 (kohn)	39	20
R3 (kohn)	1.5	2
R4 (kohn)	30	18
R5 (kohn)	1.5	0
C (nF)	1.5	2.7



+PEX_VDD [For DGPU]



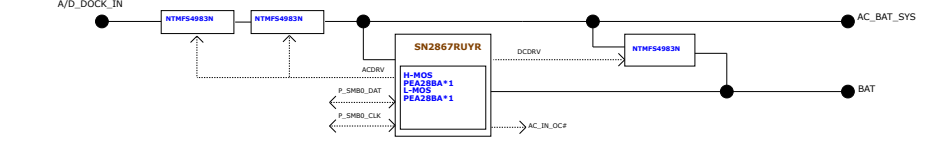
PR9221	UP1740_Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

		Project Name	Rev
		GL752VW	1.0
Title : PW_THUNDERBOLT			
Size			
B	Dept.: NB Power team	Engineer:	Joe
Date: Wednesday, September 23, 2015	Sheet	94	of 102

		Project Name		Rev
		GL752VW		1.0
Title : POWER_+VGFX_CORE				
Size B	Dept.: NB Power team		Engineer: Joe	
Date: Wednesday, September 23, 2015			Sheet 95	of 102

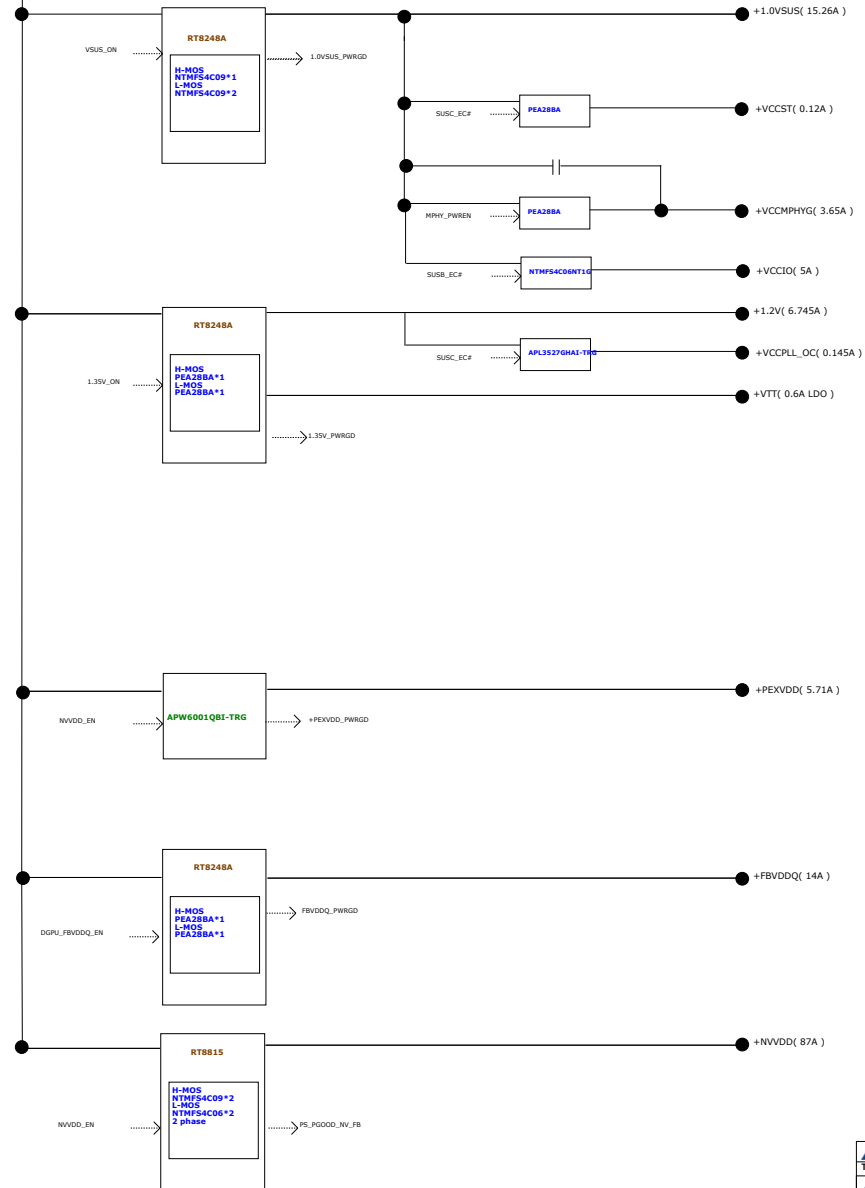
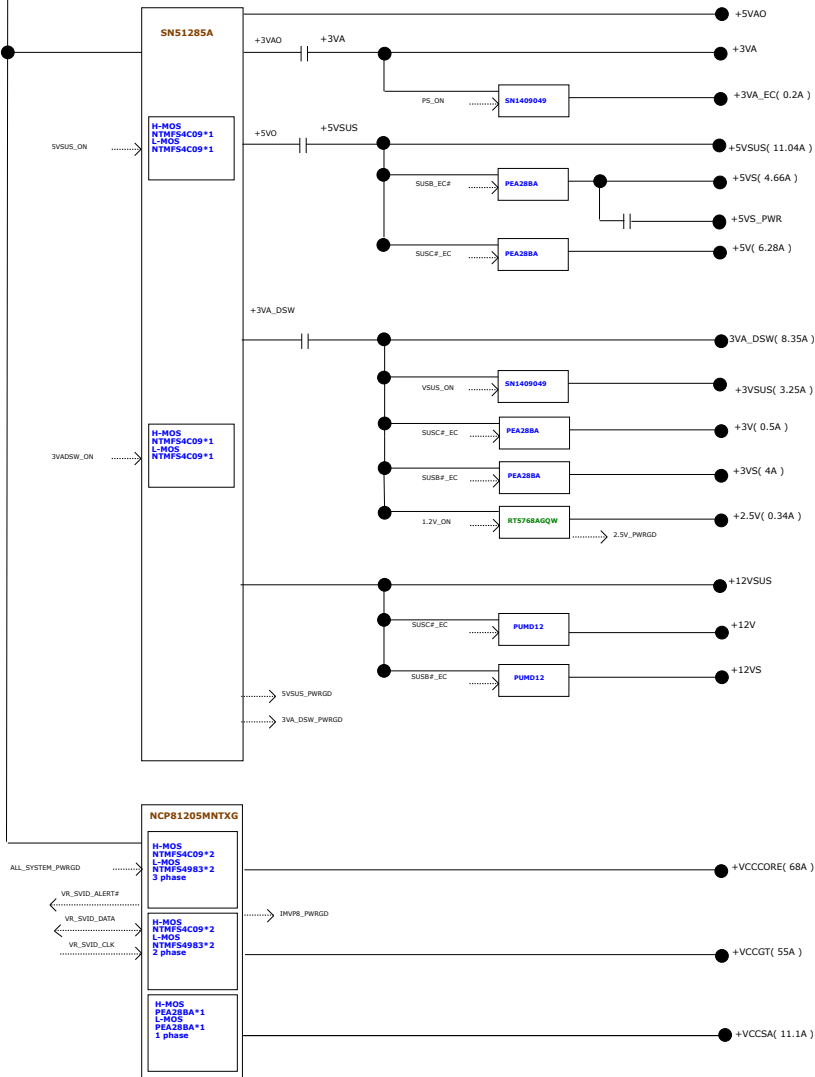
		Project Name	Rev
		GL752VW	1.0
Title : POWER_+VGFX_CORE			
Size	Dept.:	Engineer:	
B	NB Power team	Joe	
Date:	Wednesday, September 23, 2015	Sheet	96 of 102

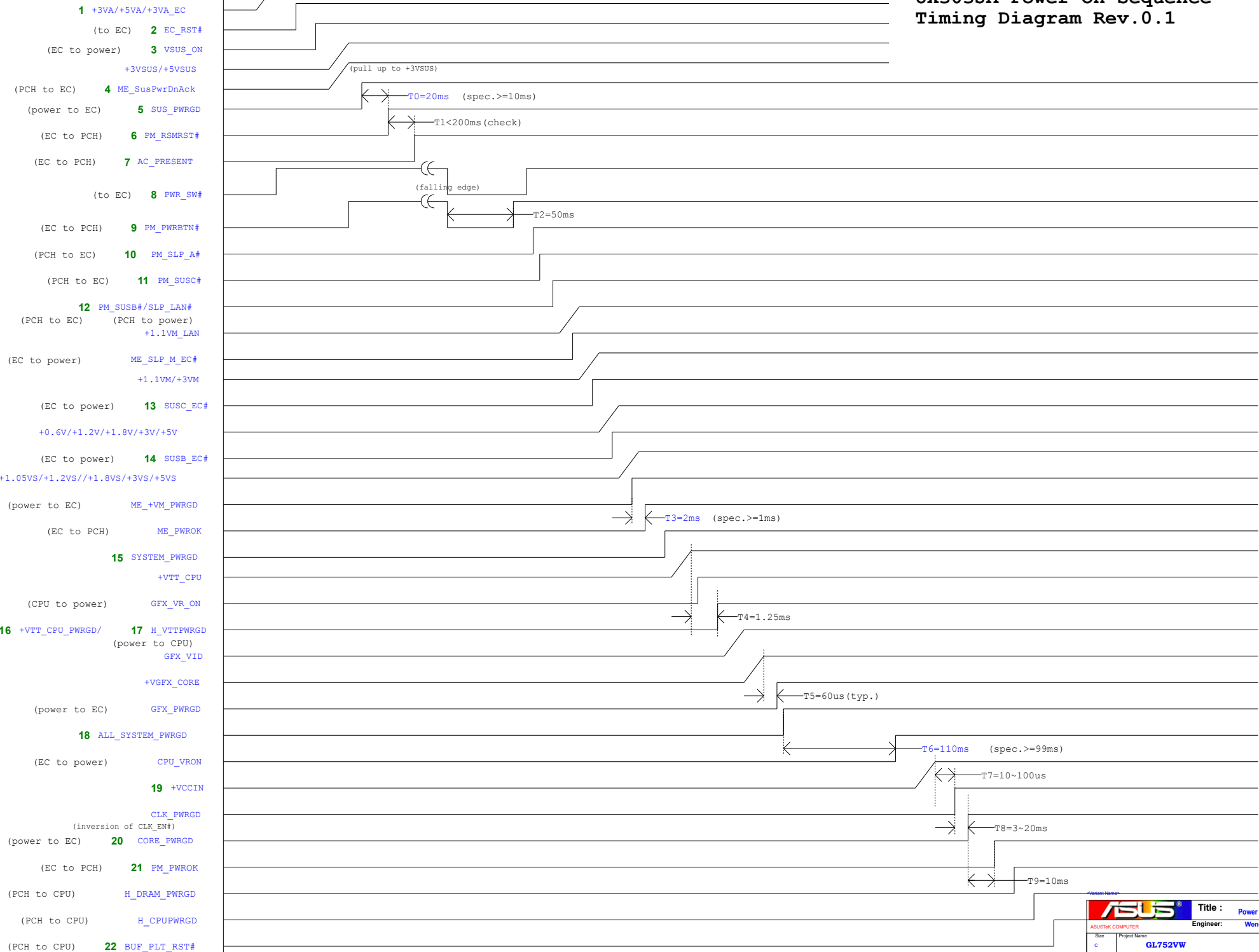
		Project Name	Rev
		GL752VW	1.0
Title : PW_OV			
Size			
B	Dept.: NB Power team	Engineer:	Joe
Date: Wednesday, September 23, 2015	Sheet	97	of 102

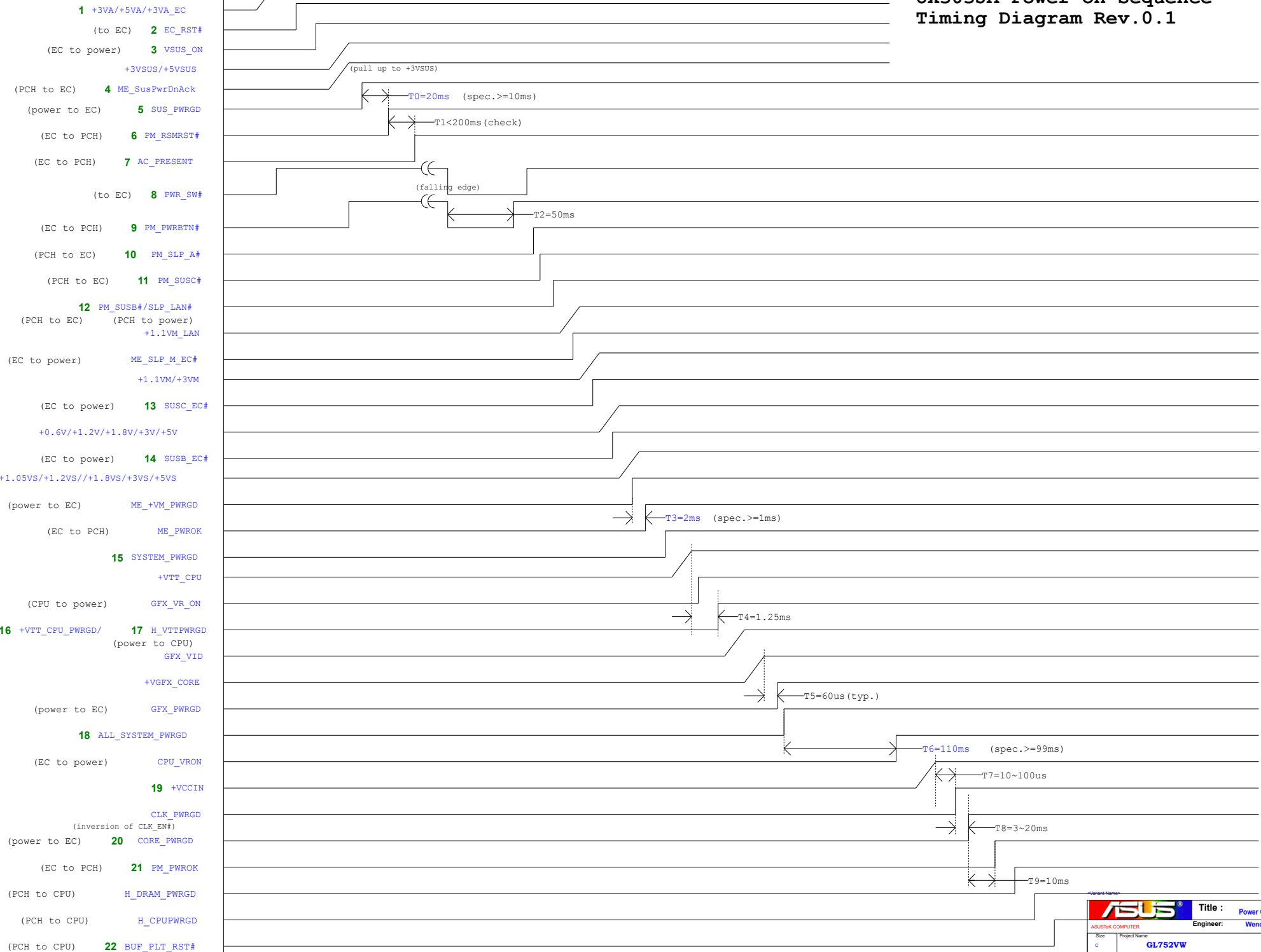


AC_BAT_SYS

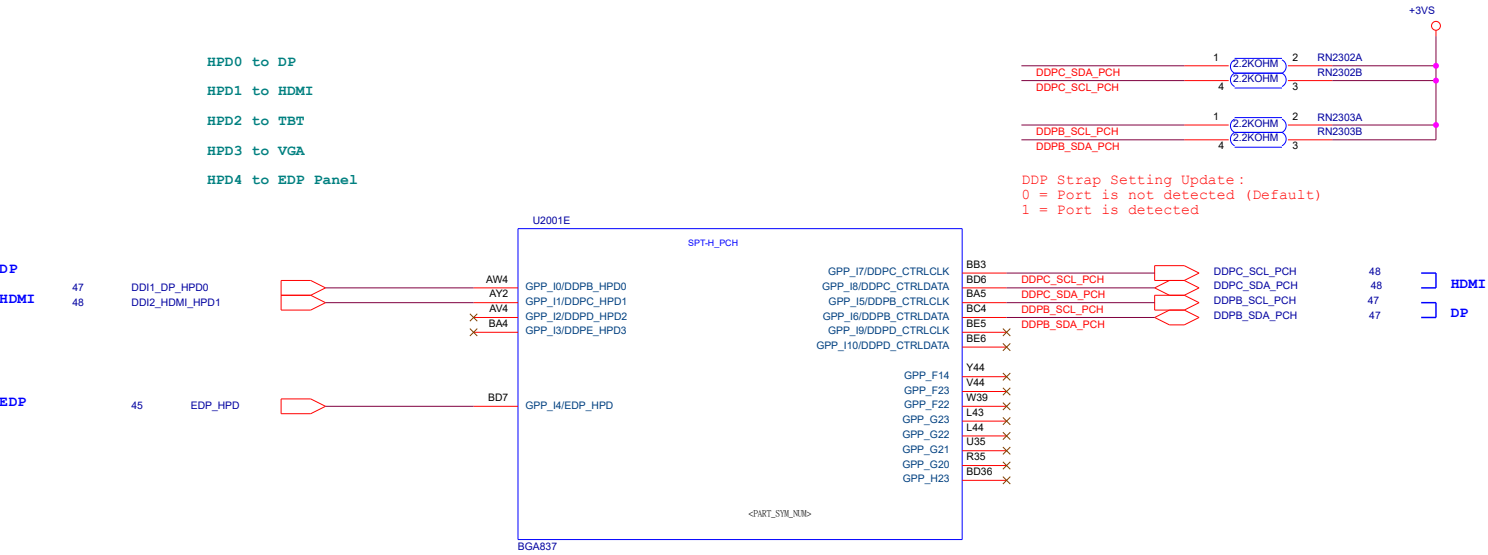
Controller
Converter
LDO
MOSFET



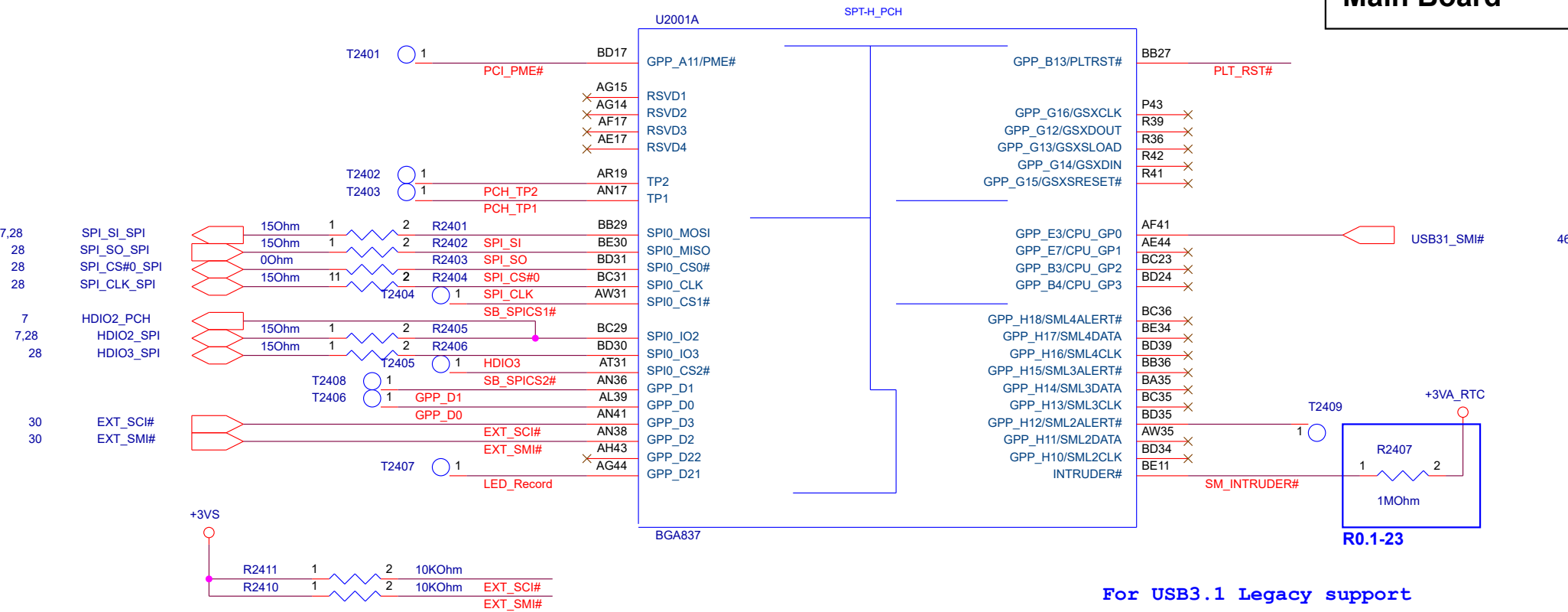




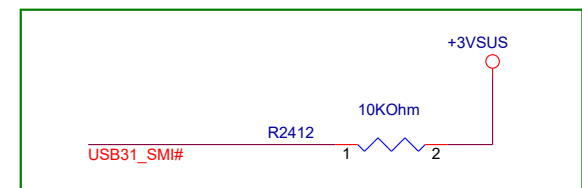
	Title :	Revision History	Rev
	Engineer:	Wendell_Lo	
L752VW			1.0



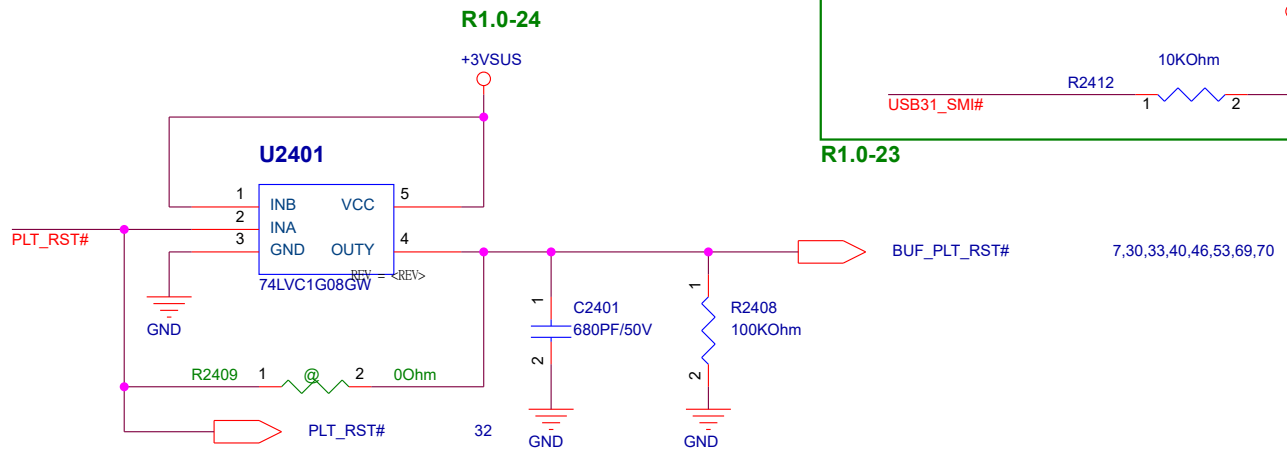
REV = <REV>



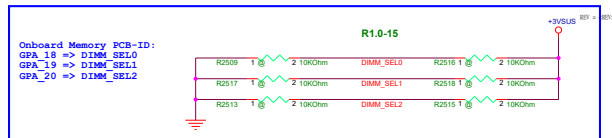
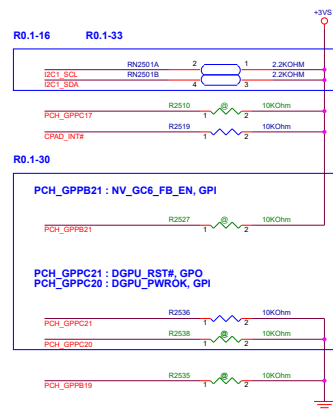
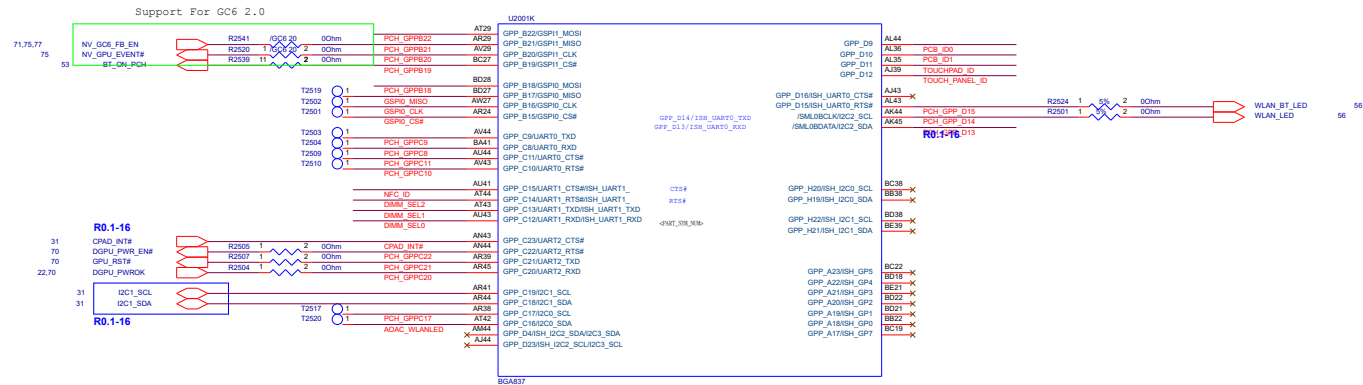
For USB3.1 Legacy support



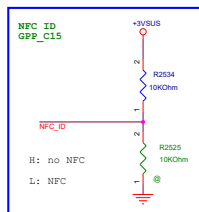
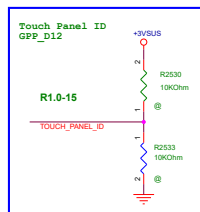
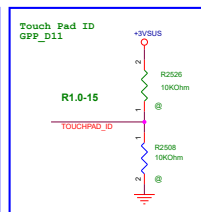
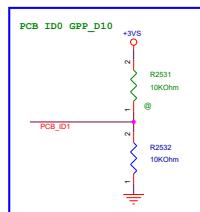
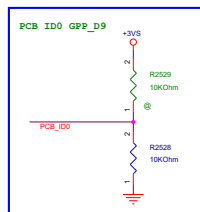
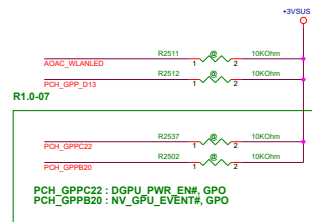
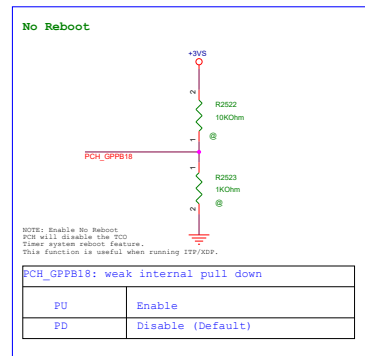
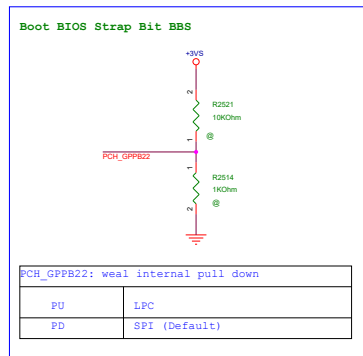
R0.1-23

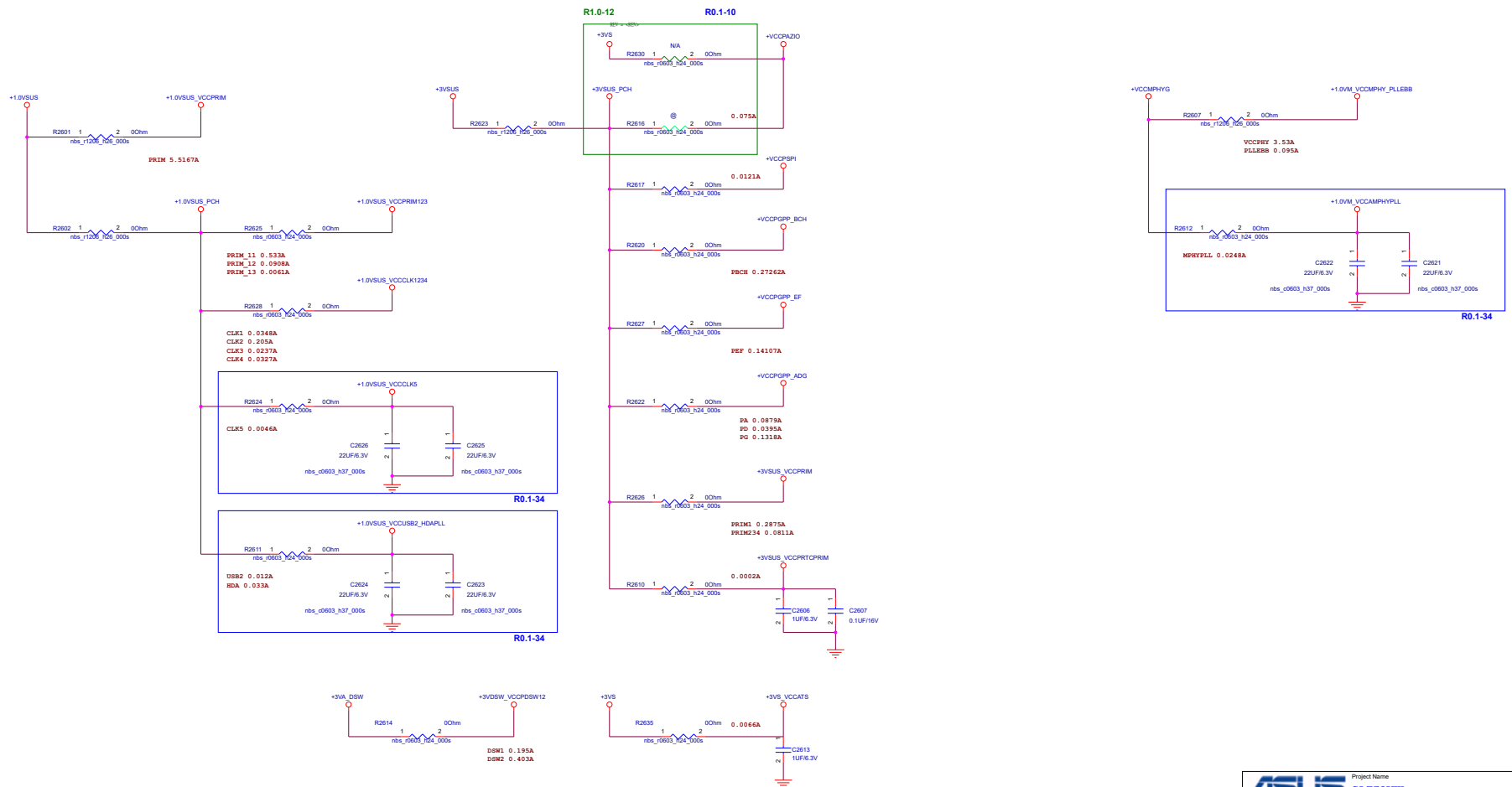
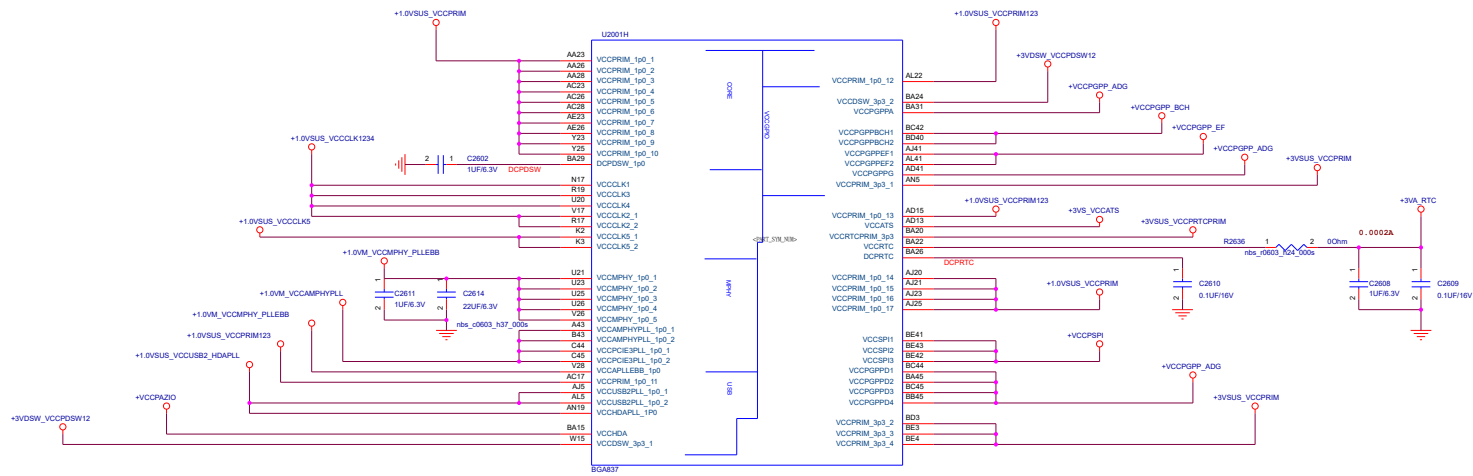


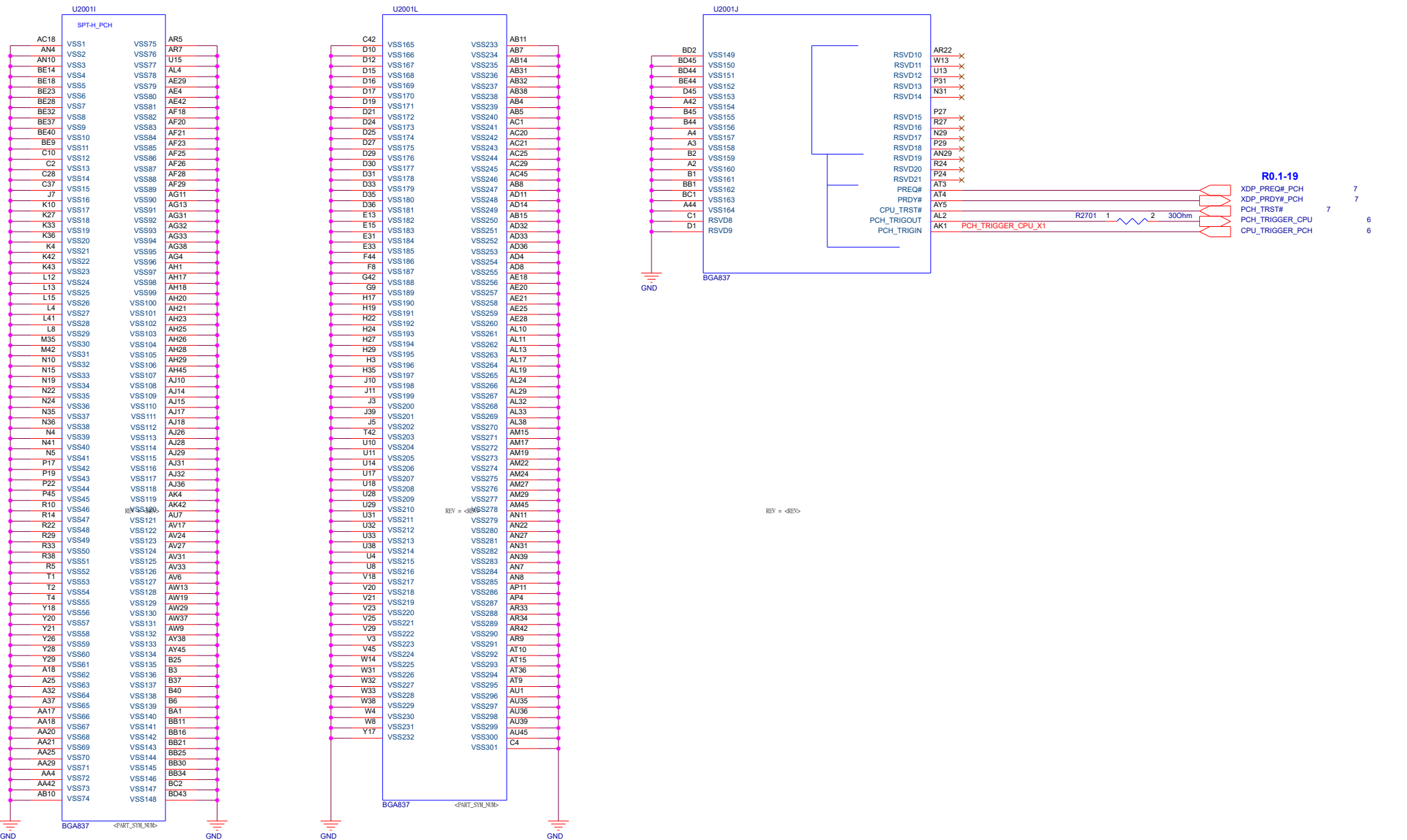
R1.0-24



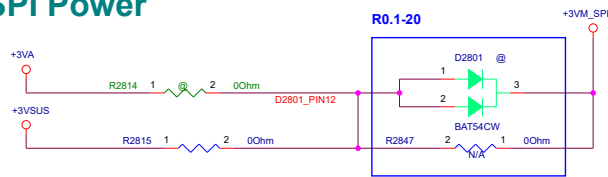
	DIMM SLOT	MEM DOWN	MEM DOWN	MEM DOWN
DIMM_SEL0				
DIMM_SEL1				
DIMM_SEL2				





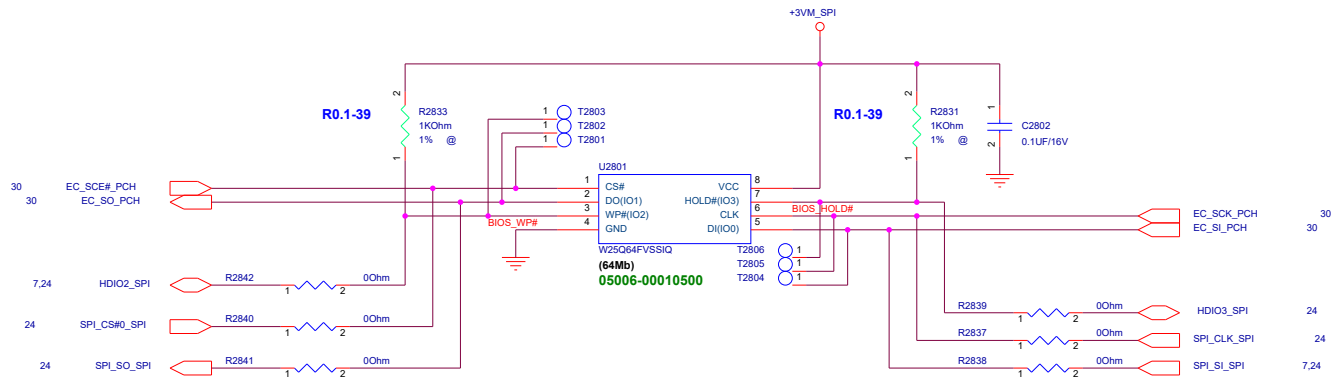


SPI Power

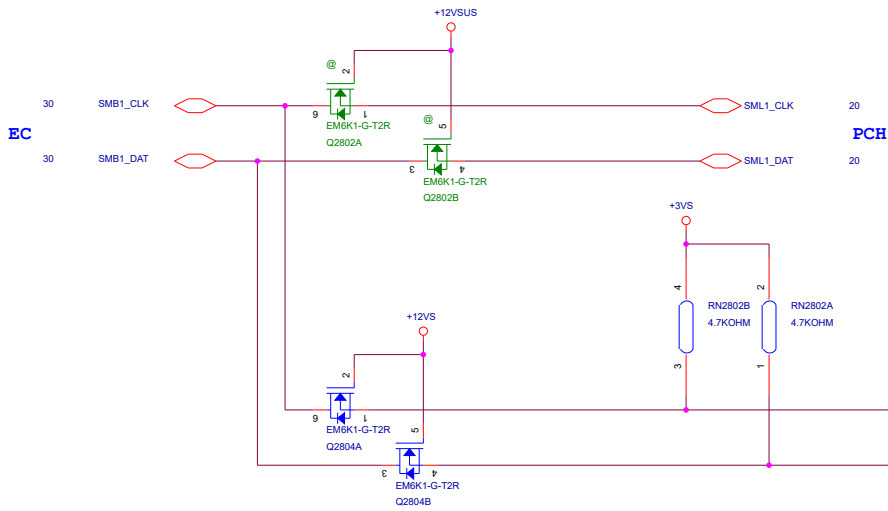


1st SPI ROM

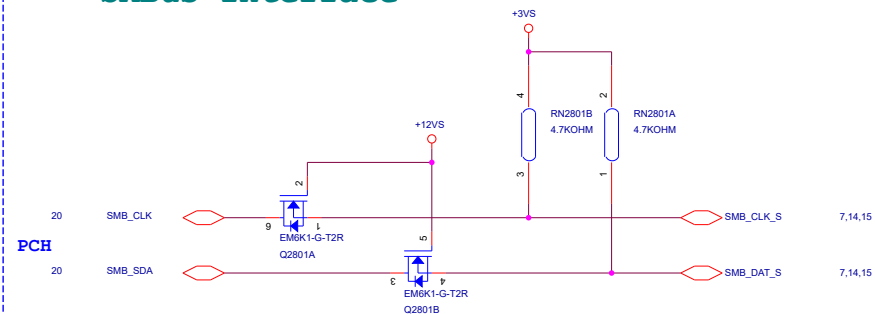
Main: 05006-00010500 (fixed quad bit)



System Management Interface



SMBus Interface



R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor

		Project Name		Rev
		GL752VW		1.0
Title : PCH-XDP				
Size B	Dept.: ASUSTeK COMPUTER		Engineer:	Wendell_Lo
Date: Wednesday, September 23, 2015			Sheet	29 of 102

Only 3V Torrence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 : 7]
GPJ [0 : 7]

Can be adjusted to
Open-Drain for port:

GPB0-GPA3
GPB0-GPB7
GPD0-GPD7
GPE0-GPE7
GPF0-GPF7
GPH0-GPH6
GPJ0-GPJ5

EC Require

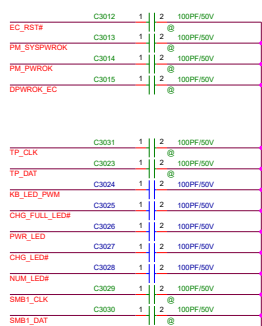
R0.1-41

ITE Version	ASUS P/N
IT8995E/AX	06037-00050400

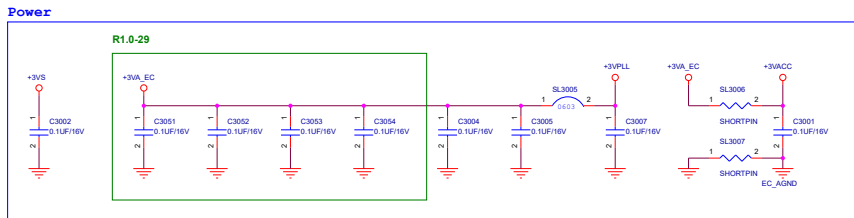
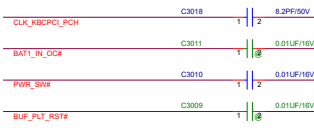
Battery

Thermal sensor

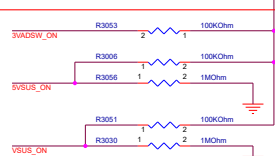
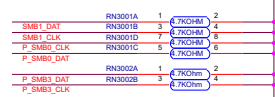
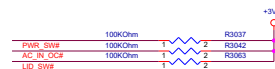
For EMI



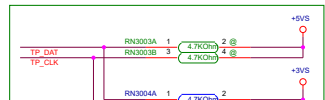
For EMI



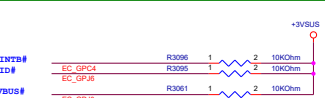
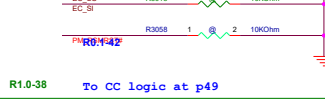
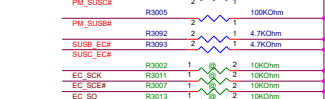
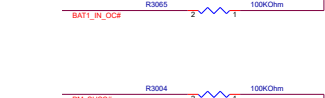
PU/PD



for load code



ClickPad Schematic



<Variant Name>

Title : CR_KBC.IT8521

Engineer: Wendell_Lo

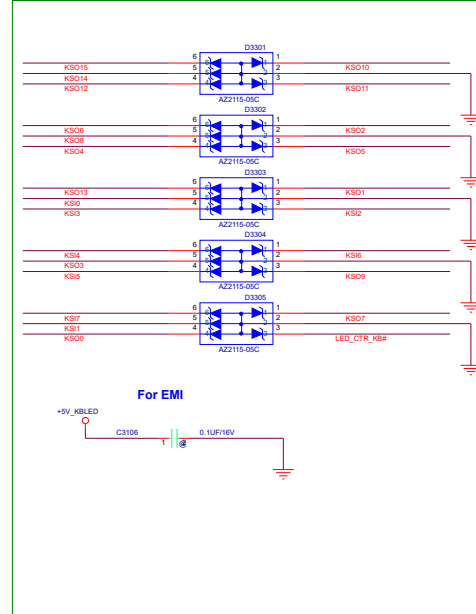
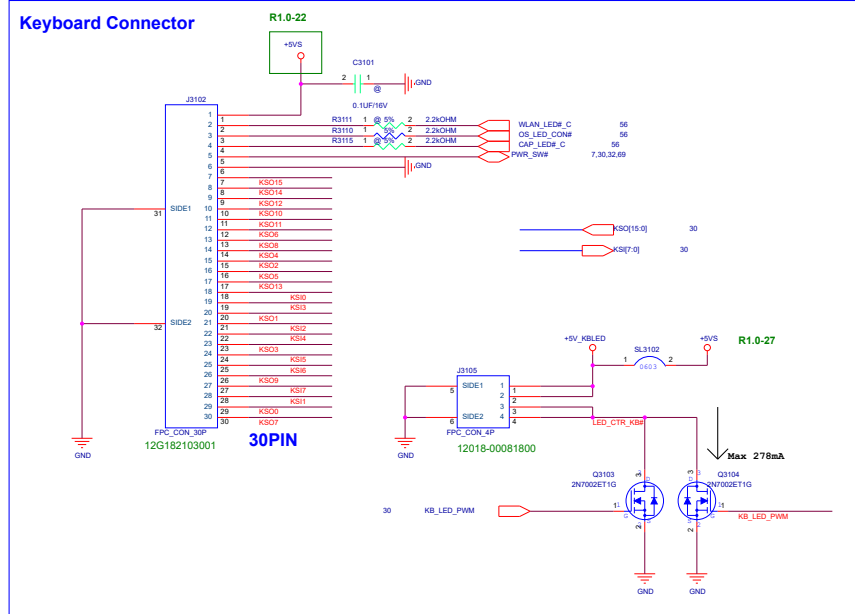
ASUSTek COMPUTER

Size Project Name

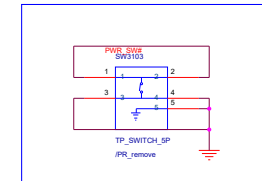
GL752VW

Date Wednesday, September 23, 2015 Sheet 30 of 102

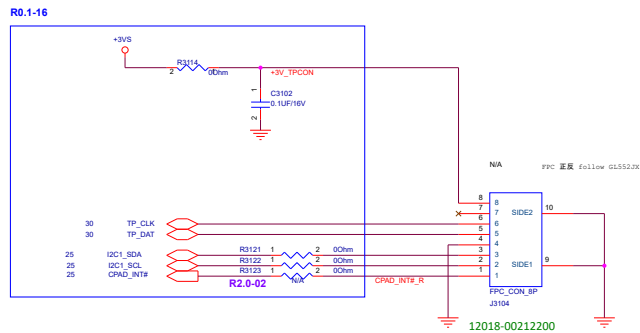
Keyboard Connector



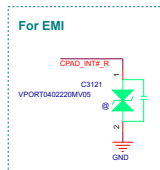
POWER button for SR



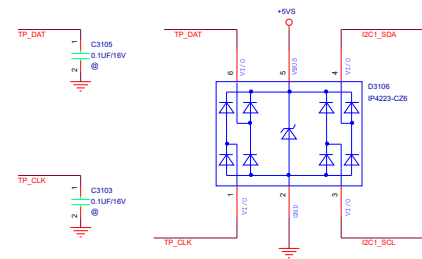
Click touch Pad Connector

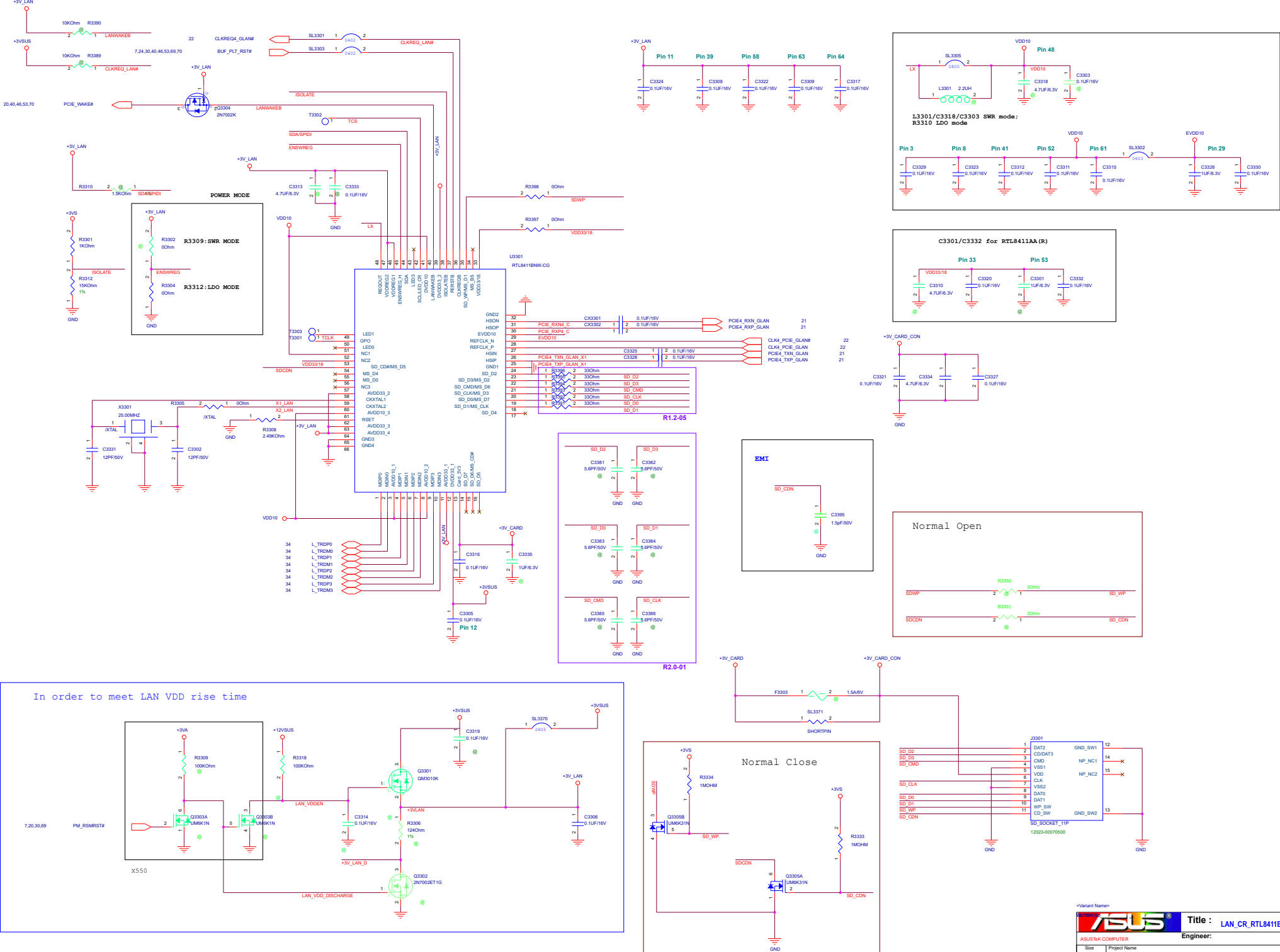


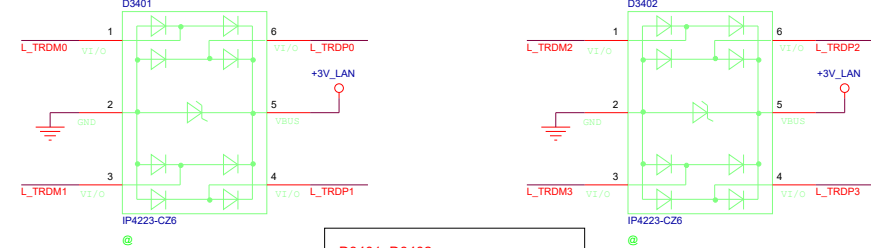
**R1.1 pin define reverse
for ME request**



Reserved for EMI

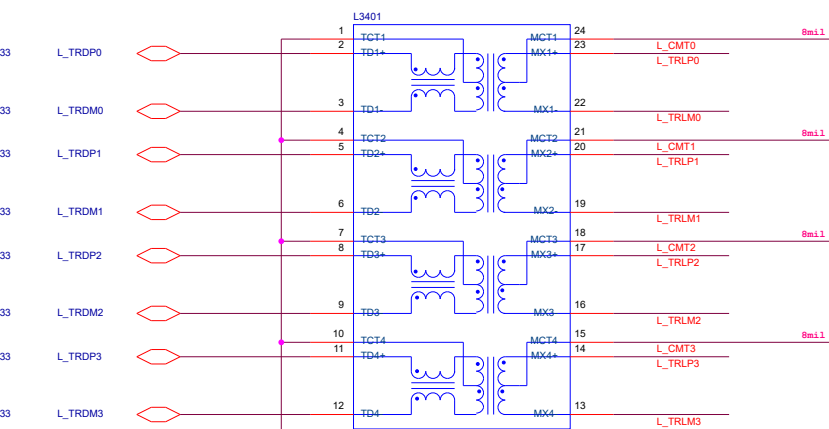




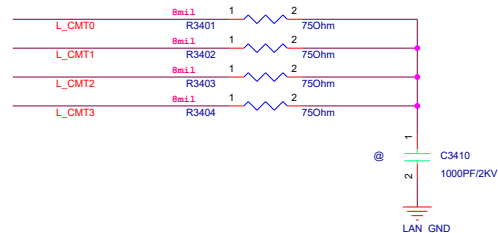


D3401, D3402
家電下鄉改用
AMAZING AZ1013-04S
07G028161010

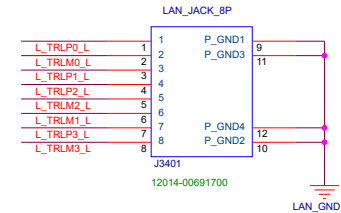
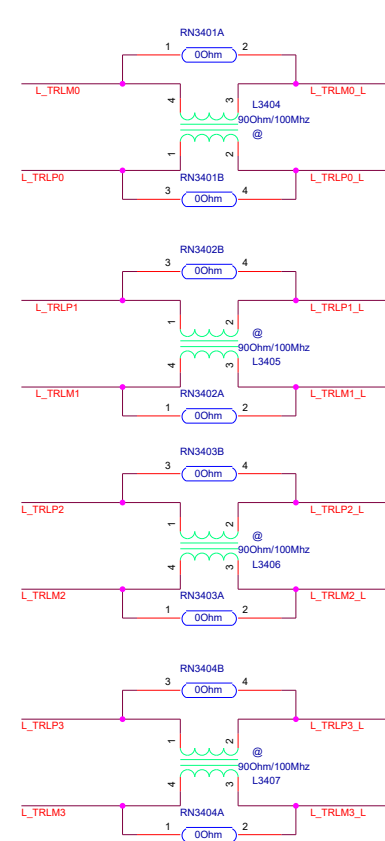
D3401, D3402 pin2
need 2 GND Vias.



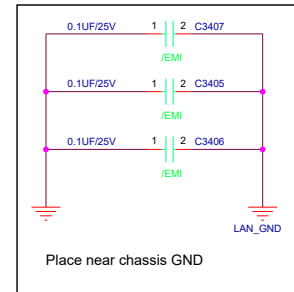
1st source: 09G051059640
2nd source: 09G051059055
3rd source: 09G051059A20
4th source: 09G051059A30



X550



Change GND TO LAN_GND FOR EMI





Title : BT_Bluetooth

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
A	GL752VW	1.0

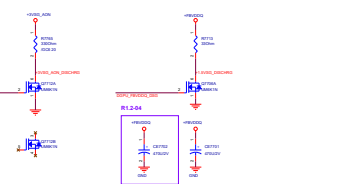
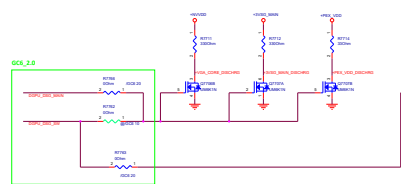
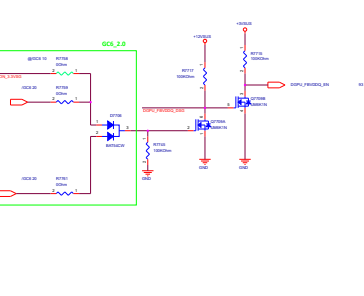
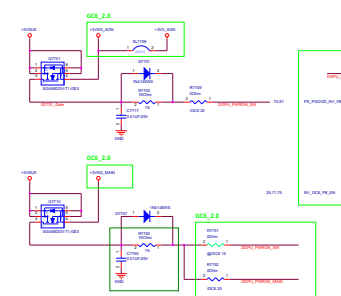
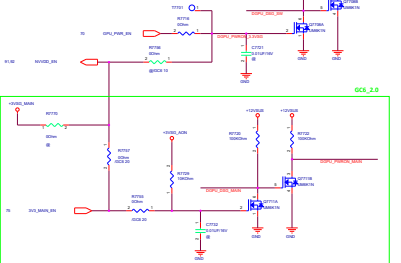
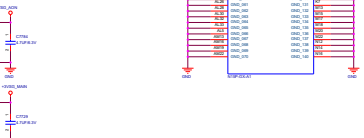
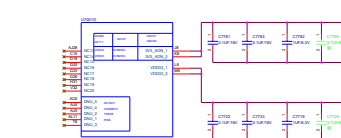
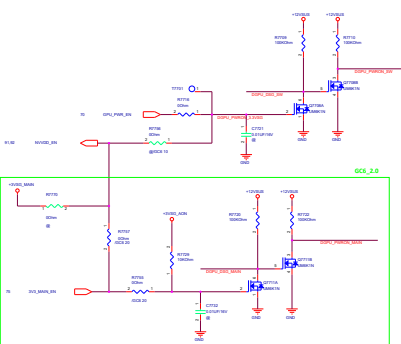
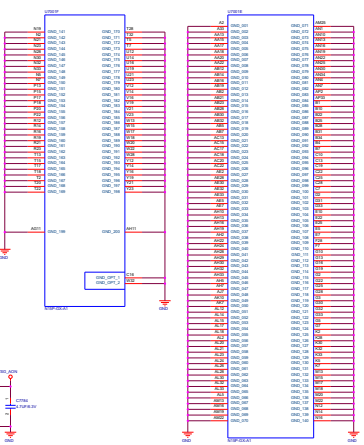
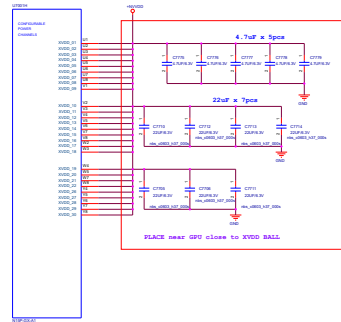
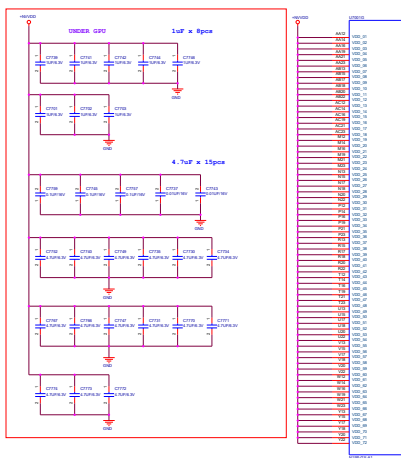
R1.0-28



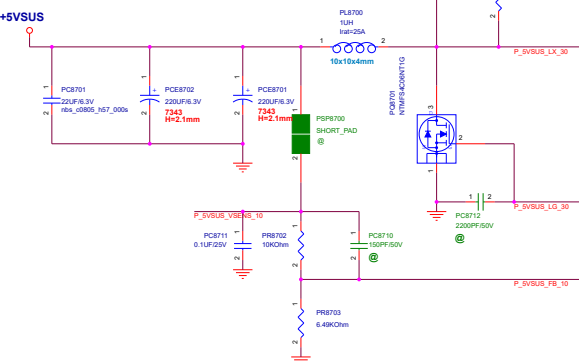
EXTERNAL MICROPHONE



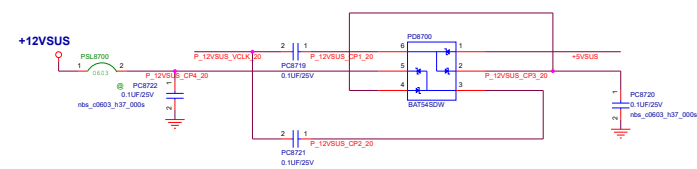
NVDD POWER AND DECOUPLING



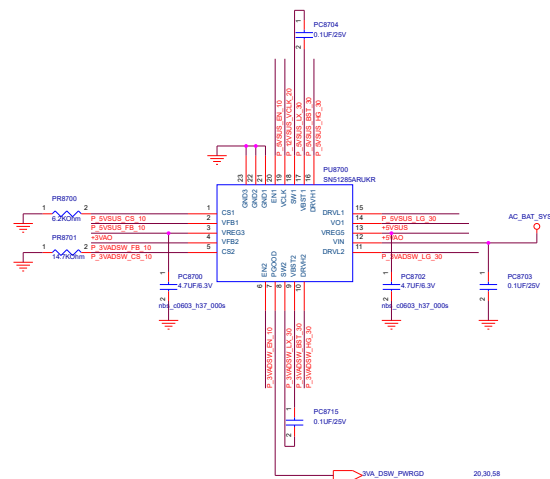
Imax= 11.04A
OCP= 17A



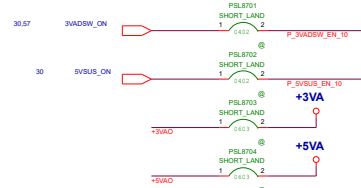
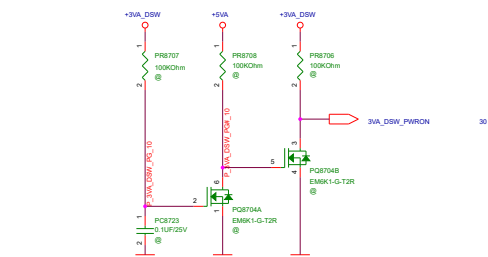
+12VSUS



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



Imax= 8.35A
OCP= 15A

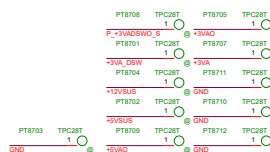


Adaptor Mode (IMVP8)

	S0	C5	S3	D53	S4	S5	S5 with USB Charger*
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.38V_ON	1	-	1	-	0	-	0
SUSC_ECR	1	-	1	-	0	-	0
SUSC_ECR	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	S1	S2	S3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
2VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSB_ECH	1	-	-	0	0	0	0
SUSB_ECH	1	-	-	0	0	0	0



+FBVDDQ [For FRAM]

